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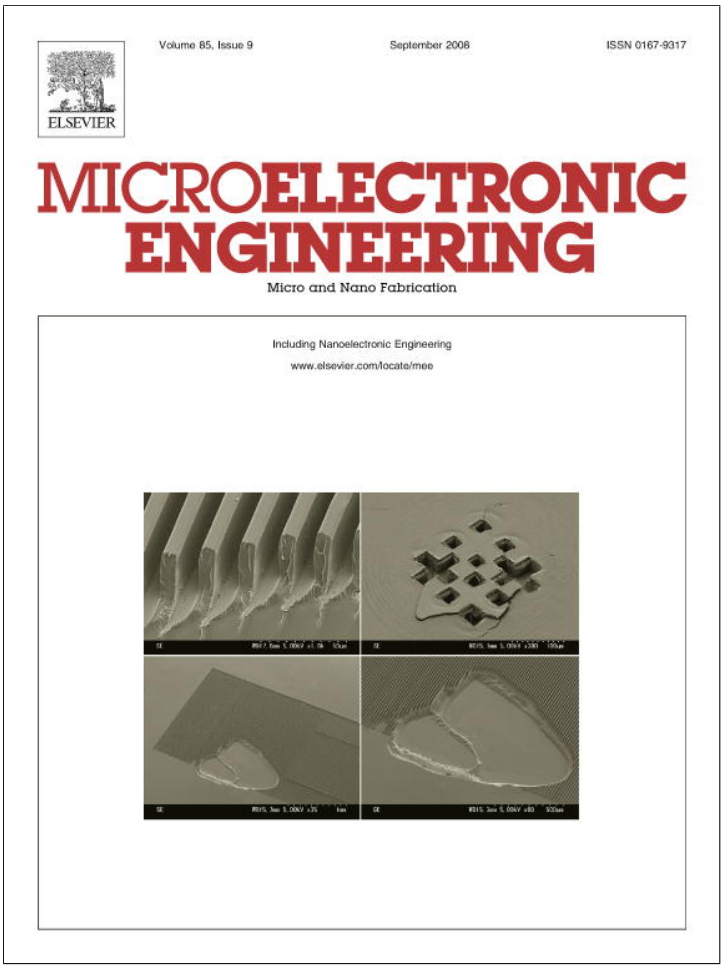

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Performance characterization of III–V power devices

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ABSTRACT

The power performance of GaAs/AlGaAs pseudomorphic high electron mobility transistors (PHEMTs) has been modeled by using the statistical Design of Experiment approach. Empirical models for the small signal gain, output power and power added efficiency have been developed. The "walk-out/in" phenomenon has been observed in the devices as a result of power measurements. The evolution of surface photovoltage spectra after RF power stress indicates accumulation of positive electrical charge in the buffer and the surface layer of the devices.

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1. Introduction

The performance of high power amplifiers (HPAs) is continually being improved in terms of power density, efficiency and gain without any reduction in reliability requirements [1–3]. Efforts in this direction have become a major driving force of device evolution with a focus on device structure and material composition [4,5].

Optimization of HEMT performance for different frequency bands and applications involves a tradeoff between device parameters. The optimization considers epi-structure, layer properties and lateral geometry, which have strong impact on the power figures of merit [6]. However, a complicated interplay between geometrical parameters, which influence the DC and RF device parameters, makes it impossible to use the "best guess approach" for exploiting the full potential of the technology. In addition, device simulators encounter significant problems in predicting actual device performance, which makes device optimization practically impossible. Under such conditions, there is a need for a robust statistical approach, based on empirical models rather than on pure "a priori" calculations [7,8].

Hot carriers play an essential role in a wide variety of modern electronic devices. Under actual operational conditions, these carriers often cause generation and/or accumulation of electrical charge at localized electronic states in the device. This is manifested when the HPA is operated under small signal and RF stress that are followed by impact ionization (II) processes [9]. These localized states are defects either in the original epi-structure or induced during the manufacturing process. The associated charges lead to a 'new' potential landscape in a device that manifests itself in shifts of the DC/RF device parameters – "walk-out/in" effects. The challenge is to develop a non-destructive technique, which may be applied at the entire chip level, making it possible to locate the accumulated charge in a given device.

Surface photovoltage spectroscopy (SPS) is a powerful tool for monitoring electric fields in HEMT structures [10]. It monitors changes in the semiconductor surface work function that are induced by absorption of monochromatic light, giving rise to surface photovoltage (SPV). The high sensitivity of this technique may be used to define whether the charge is localized at the surface or in a buffer layer.

In this paper, an empirical model based on the experimental data is being proposed. The use of the DOE (Design of Experiment) methodology for modeling output power, power added efficiency (PAE) and gain in a power transistor and HPAs, is shown. Reliable empirical models of the key device parameters have been extracted successfully, demonstrating clear and unambiguous impact of the device geometry on its performance. Power performance modeling is demonstrated and evaluated for the mature PHEMT device technology presented by HPA at 10 GHz. A methodology for direct monitoring of hot-carrier accumulated charge and walk-out/in phenomena in PHEMT devices is shown. SPS has demonstrated high sensitivity and provided a clear physical picture of the phenomena involved. The technique may be applied to any solid-state HPA technology, without losing the universality of the approach.

Section 2 describes the device structure, the experimental setup and the software tools. The measurement results and empirical modeling are discussed in Section 3. The conclusions are presented in Section 4.

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2. Experimental

A 0.25 μm gate power PHEMT was used as the basic element in this research. It included double heterostructure GaAs/AlGaAs/InGaAs MBE-grown epi-wafers, which incorporate double Si planar delta doping as a source of channel carriers (concentration – N_s), conventional alloyed AuGeNiAu, Ohmic contacts, and a double-recessed sub-micron T-gate. The vertical structure was made in two versions with a different screen layer thickness – D_S. Version EI had an 8 nm thick screen layer and version EII had a 15 nm thick screen layer.

The transistor microwave performance is usually assumed to depend on the unit cell lateral geometry. The geometrical parameters includes: gate recess (L_{wr}), drain-source spacing (L_{ds}), gate-recess spacing ($L_{wr,g}$), source-recess spacing ($L_{s,wr}$) and gate length (L_g). These key lateral layout parameters of the transistor are shown in Fig. 1. They determine the electric fields in the transistor at the desired working point under DC and RF conditions.

The statistical Design of Experiment (DOE) approach to transistor design allows deriving correlations between device performance and geometry [7,8]. Due to the complex geometry and non-linear performance of HEMTs, the derivation of an analytical dependence of device geometry on performance parameters is a very difficult task. The DOE method makes it possible to design a device matrix with different lateral and structural geometrical parameters. Thus, correlations between the geometrical parameters and measured electrical characteristics can be statistically established.

The variables for the device matrix were based on a combination of the key lateral layout parameters of the power HEMT. The two-level device matrix makes it possible to model the electrical characteristics of the matrix taking into account the entire first and second order effects. Without loss of generality [11,12], the following ranges of five key layout parameters have been chosen in our case to optimize a 10 GHz HPA: L_g – 0.2–0.3 μm, L_{wr} – 1.4–1.7 μm, L_{ds} – 3–3.5 μm, $L_{wr,g}$ – 0.4–0.6 μm and $L_{s,wr}$ – 0.7–0.9 μm. The device matrix has been manufactured and measured on wafers with two different carrier concentrations ($N_s = 3 \times 10^{12}$ and 3.2×10^{12} cm^{-2}, respectively) from different lots.

To evaluate the transistor power performance, the output power, gain and power added efficiency figures of merit have been used. These figures make it possible to compare the transistor performance and select the best device for a given specific application.

The general form of the equation describing the effect of the model terms (layout dimensions) on the modeled parameters (measured values) is given by

$$\Phi = A_0 + \sum_n A_n \cdot P_n + \sum_{n,m} A_{nm} P_n P_m, \quad (1)$$

Where Φ the modeled parameter, $P_{n,m}$ are the model terms and $A_{n,m}$ are correlation coefficients.

The power measurements were performed using electromechanical tuners. On-wafer load–pull measurements were used to obtain the characteristics of the PHEMT at 10 GHz in several operational DC ranges: V_{ds} = 5–9 V; V_{gs} = −1.1 to −0.6 V, for several input/output impedances (the typical source-drain breakdown voltage (V_{br}) is higher than 18 V). The P_{in}–P_{out} characteristics of the PHEMTs were measured in the range of output impedance: R = 10–35 Ω; jX = −12–+18 Ω, which covers the region of the optimal impedances. The load tuners were selected to provide the best matching for maximum power performance, corresponding to ~2–3 dB gain compression under actual operational conditions. The setup consisted of a number of basic blocks: DC power supply, RF Source, passive load–pull, and a computer. Fig. 2 shows a schematic representation of the setup.

A detailed description of the SPS technique and its applications may be found in Ref. [13]. This technique has been successfully applied for characterization of novel structures and devices [14–18]. SPS makes it possible to monitor the evolution of the electric field distribution within a device as a function of the operational conditions. With SPS, the change in the contact potential difference (CPD) between a reference gold electrode and a semiconductor surface is monitored as a function of photon energy. The total signal is a combination of signals, which are a function of the light absorption and electric fields in all the structure layers penetrated by light. The two oppositely directed electric fields in the buffer and Schottky layer define the potential profile of the structures. Since the CPD is sensitive to the electric field direction, the CPD signals resulting from the buffer and Schottky layers are of opposite signs (positive from the buffer and negative from the Schottky layer).

Absorption of light in the quantum well (QW) creates electron–hole pairs. While electrons are confined to the QW by the fields in the buffer and Schottky layers, holes are swept by the electric field in the buffer or in the Schottky layer direction, contributing to signals with opposite signs.

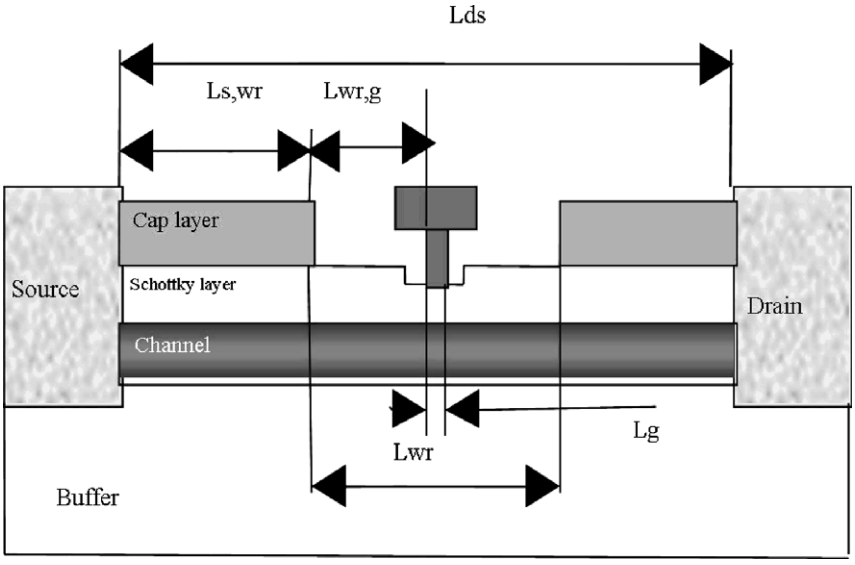

Fig. 1. Schematic diagram of the double-recessed HEMT.

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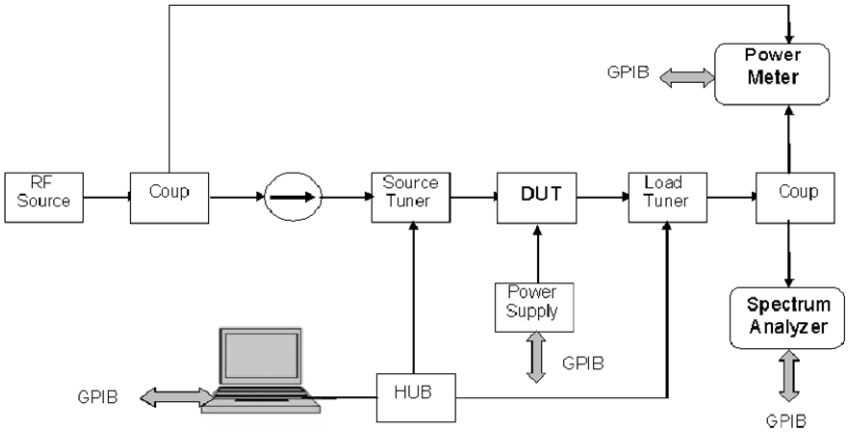

Fig. 2. Schematic representation of the load–pull measurement setup.

For each transistor under test, output power, efficiency, gain, gate/drain currents were collected. All electrical measurements were performed on the wafer using a HP 4155C semiconductor analyzer and an 8510C network analyzer and a passive load–pull. The statistical analysis of the data was carried out using SAS software (JMP 5.0). The SPS measurements were performed in air using a commercial Kelvin probe unit (Besocke Delta Phi, Germany). The optical system consisted of a 250-W tungsten–halogen lamp, a double monochromator (Oriel, USA) and a set of band pass filters to avoid second order harmonics. The measurement sensitivity was about 1 mV and the light intensity was at the order of 10 $\mu W/cm^2$ at a wavelength of 750 nm. Neutral density filters controlled the light intensity.

3. Results and discussions

Fig. 3 shows the results of the load–pull tests in terms of P_{out} as a function P_{in} for the different devices. Devices with 0.3 mm gate periphery demonstrated a maximum output power 900 mW/mm when the gate bias was set to −0.9 V and the drain bias to 8 V. The spread in output power at a given incident power P_{in}, reflects the impact of the device geometry and carrier concentration on the power performance. For instance, at incident power P_{in} = 18.5 dBm, the output power varied between 650 mW/mm and 900 mW/mm. The following empirical formula was extracted from the measured data:

$$P_{out}[\mathrm{mW/mm}] = -723 + 6.17e^{-10} \cdot N_s - 860 \cdot L_g + 143 \cdot L_{wr,g} - 33 \cdot L_{s,wr} - 104 \cdot L_{wr} \quad (2)$$

The output power is proportional to the product of the maximal current and the breakdown voltage ($I_{max} \times V_{br}$) defining the power swing. The breakdown voltage is marked by a sharp increase in the gate/drain current [19,20] and is defined by a direct measurement, where the negative gate current (I_g) reaches a magnitude of 1 mA/mm. The increase in I_g is due to minority carriers (holes), which are generated by the impact ionization process. This process entails free carrier generation in the transistor. The output power is affected by N_s and L_g, which define I_{max}: Increasing N_s and decreasing the gate length contribute to increasing saturation current and P_{out}. The layout parameters $L_{s,wr}$ and $L_{wr,g}$ define the electrical field in the drain-source region, becoming a limiting factor of V_{br}. Therefore, an increase in the gate-recess distance will lead to an increase in V_{br} and consequently to an increase of output power. The recess width (L_{wr}) impacts the output power through two competing phenomena: On the one hand, a reduction in L_{wr} leads to an increase in I_{max} due to reduction in the open surface area; On the other hand, a reduction in W_r leads to a decrease in the breakdown voltage (V_{br}) of the device due to the increasing maximal electrical field. Since the relative impact of L_{ds} is small, it is not included in the equation.

Fig. 4a shows the quality of the model. The model, including only the main effects, predicts the measured values by 88%. Therefore, for the sake of simplicity, the second order effects can be excluded without significant loss of information.

The following analysis is based on data collected from a single wafer. Therefore, only the layout effect is estimated. The following empirical formula for small signal gain has been extracted from the measured data:

$$\mathrm{Gain\ (dB)} = 17 - 5 \cdot Lg \quad (3)$$

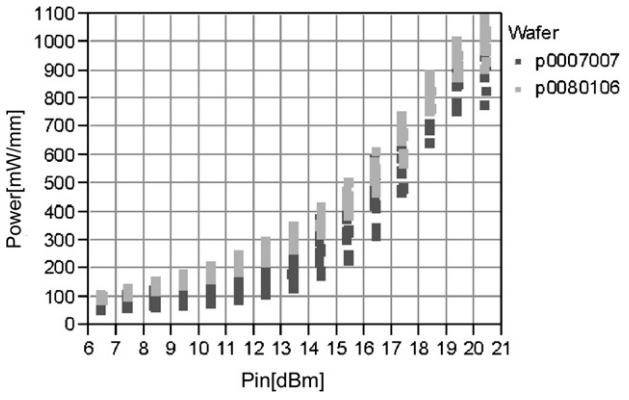

Fig. 3. Output power – P_{out} [mW/mm] as a function of input power – P_{in} [dBm].

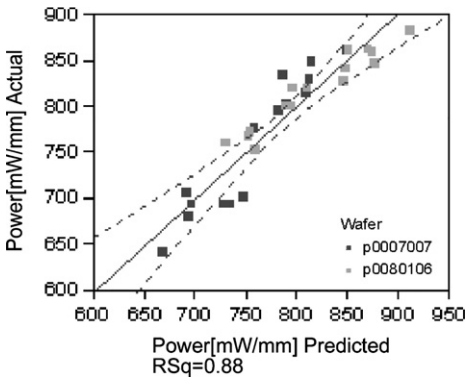

Fig. 4a. Correlation between measured and predicted P_{out} values.

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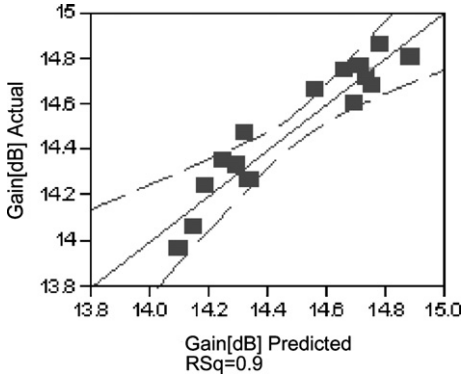

Fig. 4b. Correlation between measured and predicted small signal gain values.

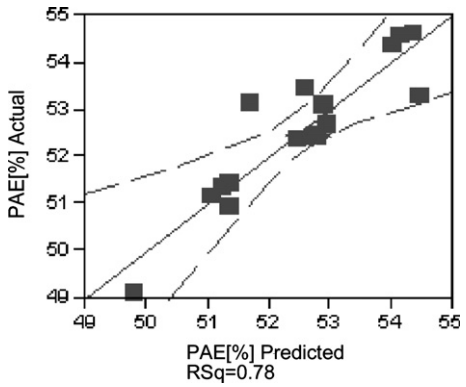

Fig. 4c. Correlation between measured and predicted PAE values.

The small signal gain shows dependence on gate length (L_g), as should be expected from basic considerations [21]. A decrease in L_g from 0.3 μm to 0.2 μm causes improvement of the gain by 0.5 dB.

Fig. 4b shows the quality of the model. The model, including only the main effects, predicts the measured values by 90%.

The following empirical model for the power added efficiency (PAE) has been extracted from the measured data:

$$PAE(\%) = 61 - 10 \cdot L_g + 1.4 \cdot L_{ds} + 2.9 \cdot L_{wr,g} - 1.5 \cdot L_{s,wr} - 7 \cdot L_{wr} \quad (4)$$

The PAE shows considerably lower sensitivity to the layout parameters. The accumulated change in PAE is about 6% for devices with various layouts. The PAE is mostly affected by L_{wr}, $L_{s,wr}$, $L_{wr,g}$ and L_g. The effect of the first three parameters is related to the output power, while the effect of L_g originates in the gain behavior of the device.

Fig. 4c shows the quality of the model. It predicts the measured values by 83%. Therefore, for the sake of simplicity, second order effects can be neglected without significant loss of information. As expected from the empirical model, there is a positive correlation between these parameters.

Fig. 5 shows the correlation between the output power, PAE and the small signal gain. A number of devices showed recoverable walk-out phenomena, where the output power changed during power measurements, reaching saturation values that were different from the initial ones. A set of SPS and RF measurements has been carried out to monitor changes in the potential profile. The changes in SPV spectra during an experiment may manifest itself in terms of charge accumulation at imperfections in the structure. The electric measurements were done in three steps: 1. Small signal conditions (a constant drain-source voltage of $V_{DS} = 2$ V); 2. Large signal conditions, $V_{DS} = 8$ V; 3. Small signal conditions,

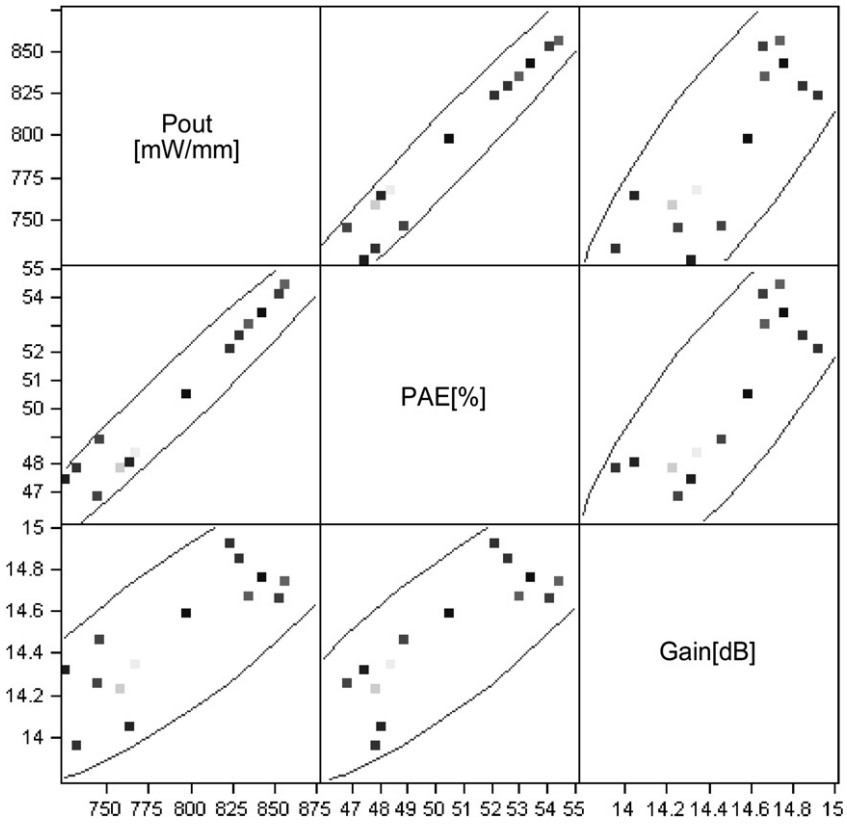

Fig. 5. Correlation between output power, PAE and small signal gain.

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V_{DS} = 2 V. At each step, the drain-source current and transconductance were measured as functions of the gate-source voltage.

Fig. 6 shows *I–V* curves under small signal conditions for a PHEMT on the epitaxial structure EI in step 1 (empty squares, triangles and circle) and step 3 (filled squares, triangles and circle). The threshold voltage became more negative after large signal conditions had been applied. Under these large signal conditions a negative gate current was measured, which could be attributed to impact ionization [1,2] in the device. Impact ionization leads to significant generation of electron–hole pairs and these excess carriers contribute to the negative gate current. For *I–V* measurements of version EII, the same negative gate current is observed under large signal conditions but there is no difference between *I–V* curves under small signal conditions.

The CPD spectrum is measured before each electrical measurement step, i.e.: 1. before any voltage application; 2. after a small signal measurement; 3. after a large signal measurement. The evolution of SPV spectra under the above experimental conditions for a PHEMT on the epitaxial structure EI, is presented in Fig. 7. The first "peak" indicates interplay of signals from the buffer and Schottky layers as a result of light absorption in the channel (InGaAs). In the case demonstrated in Fig. 7, the signal from Schottky layer is dominant, which results in a change in the CPD. When the signal from the Schottky layer is saturated, the total CPD changes polarity.

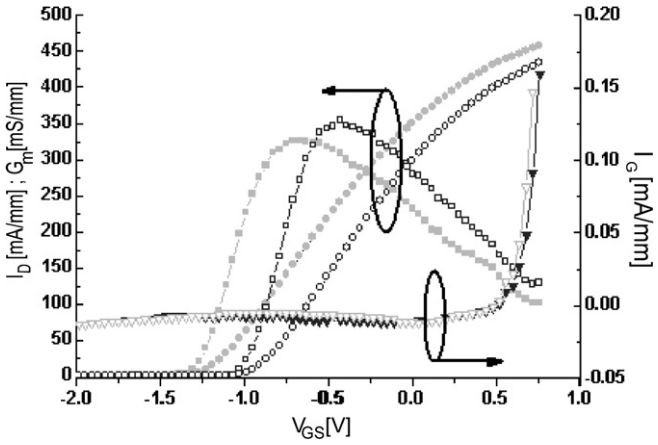

Fig. 6. *I–V* Curves under small signal conditions for a PHEMT on the epitaxial structure EI.

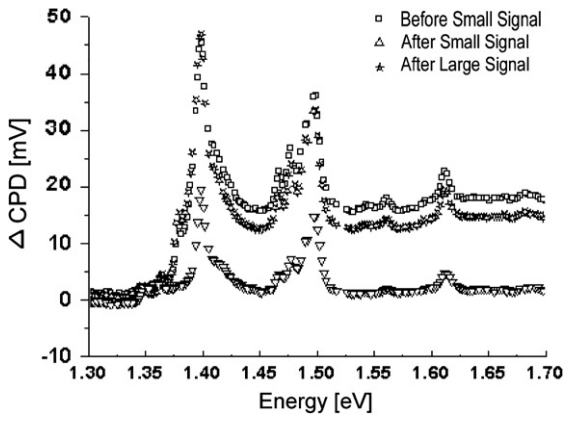

Fig. 7. Evolution of CPD spectra of a PHEMT on structure EI under various operational conditions: Squares – bare device; triangles – after exposure to small signal conditions; stars – after impact ionization.

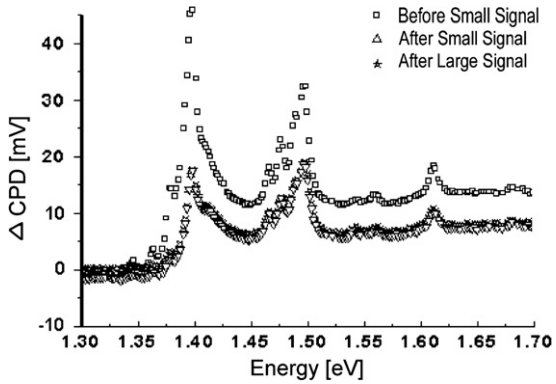

Fig. 8. Evolution of CPD spectra of a PHEMT on structure EII under operational conditions: Squares – bare device; triangles – after exposure to small signal conditions; stars – after impact ionization.

The shape of the spectra for the three curves is the same while the peak values are different: The highest absolute value of the first peak for the bare device (squares in Fig. 7) is significantly reduced during small signal measurements. The device is driven to an open state, where the device surface is exposed to hot electrons. These carriers are trapped at the surface, which becomes more negative as compared to the pristine device, reducing the SPS signal (triangles). The highest absolute value of the first peak increases after exposure to hot electrons and holes in step 3 (stars). The ensuing large signal measurements induce electron–hole generation, whereby the holes are driven by the electric field towards either the surface or/and the buffer. Trapped holes at the surface states make the device surface more positive. The evolution of the SPS spectrum of structure EII is similar to that of EI for the first two steps, although there is no change in amplitude between measurements at steps 2 and 3.

Fig. 8 shows the CPD spectra of structure EII. The same electron trapping phenomena appear after small signal measurements. Due to the better screening capabilities in the epi-structure of version EII, there is no change in the SPS signal after large signal RF measurements.

Thus, the SPV spectrum evolution indicates significant imperfections, which are caused by some steps in PHEMT manufacturing process. The imperfections behave both as electron and hole traps. Planned variations in the epi-structure may reduce the effect of the accumulated charge at the device surfaces. SPS may be used as a quality assurance tool in such production processes.

4. Conclusions

Extensive measurements and analyses of the output power, small signal gain and PAE of power PHEMTs have been carried out and corresponding empirical models have been presented. These models show good correlation with the experimental measurements and highlight the pronounced impact of the device layout parameters on the output power, which correlates with the maximal current I_{max} and the device breakdown. The small signal gain shows a clear dependence on gate length (L_g), as expected from first principles. The PAE shows considerable lower sensitivity to the layout parameters.

A systematic evaluation of DOE as a powerful tool for power performance optimization through empirical modeling has been presented. Also, a methodology for directly monitoring walk-out phenomena in HEMT devices has been demonstrated.

The evolution of photovoltage spectra indicates the presence of two types of traps for electrons and holes in PHEMTs, which are

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induced during the manufacturing process. These traps are populated during impact ionization, which occurs during power measurements.

The models may be used to predict the output power, small signal gain and PAE of a device and to optimize device performance for a chosen application. They can also provide an additional degree of freedom for sensitivity analysis at the circuit simulation level. The models can be integrated into the PHEMT model that is used in the circuit simulation software. SPS can be used as a powerful monitoring tool in manufacturing processes in order to find out the extent of "walk-out/in" effects in the device.

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