Characterization of Transient Gate Oxide Trapping in SiC MOSFETs Using Fast I–V Techniques

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***Abstract*—Threshold voltage and drain current instabilities in state-of-the-art 4H-SiC MOSFETs with thermal as-grown SiO_2 and NO-annealed gate oxides have been studied using fast I–V measurements. These measurements reveal the full extent of the instability underestimated by dc measurements. Furthermore, fast measurements allow the separation of negative and positive bias stress effects. Postoxidation annealing in NO was found to passivate the oxide traps and dramatically reduce the instability. A physical model involving fast transient charge trapping and detrapping at and near the SiC/SiO_2 interface is proposed.**

***Index Terms*—Annealing, charge carrier processes, reliability, silicon carbide, transient trapping.**

I. Introduction

4H-SILICON carbide (SiC) possesses excellent material properties for high-temperature, high-frequency, and high-power applications. It has a wide band gap (3.26 eV), a high thermal conductivity (more than twice higher than that of Si), a high critical field (2.2 versus 0.25 MV/cm for Si), a high saturated drift velocity (higher than that of GaAs), and high thermal stability; it is chemical inert; and it forms a native oxide. However, the reported channel mobility values of SiC MOSFETs are extremely and unacceptably low (below 10 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$). This poor device performance is attributed to the high density of traps at and near the SiO_2/SiC interface [1]. Electron energy loss spectroscopy studies have shown a carbon-rich transition layer expanding several nanometers into the oxide [2]. This transition layer may be the reason for the high trap density. Postoxidation annealing of the gate oxide in nitric oxide (NO) or nitrous oxide (N_2O) was found to successfully and considerably improve the device performance, and peak field-effect mobility values of up to 50 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ have been reported [3]. Recently, a record peak field-effect mobility of 150 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ has been achieved after performing the oxidation process in the presence of alumina [4]. It has been found that the higher mobility was due to reduction of the near-interface trap density by sodium contamination [5]. Sodium may be incorporated during oxidation by using alumina furnaces or by deliberate sodium contamination of the SiC prior to oxidation. Unfortunately, the existence of mobile charges in these MOSFETs makes them unstable above room temperature and prevents practical use of this method for device manufacturing.

In spite of the considerable progress in device performance, reliability may be another limiting factor for the introduction of SiC MOSFETs in commercial power devices. One of the major reliability concerns is the instability of the threshold voltage in MOSFETs and, similarly, of the flat-band voltage in capacitors under normal operation conditions. This instability is attributed to transient trapping of channel electrons in interface and bulk oxide traps. Potbhare *et al.* successfully modeled this instability as a result of minority carrier recombination with interface trap states [6]. This phenomenon has been studied using dc sweep measurements (measurement times of 0.1–1 s) [7], [8]. However, due to its transient nature, it is important to study this phenomenon using as fast an I–V measurement technique as possible. In this paper, V_{TH} instability has been studied using fast I–V measurements.

Field-effect mobility is a figure-of-merit for comparing device performance. Field-effect mobility is extracted from the device I–V transfer characteristics. The disadvantage of this mobility measurement technique, in contrast with Hall effect mobility measurements, is that it cannot separately measure the intrinsic mobility from the channel carrier density. An increase in both carrier density and intrinsic mobility can explain the superior NO-annealed field-effect mobility. Hall effect mobility measurements [9] on devices with thermal as-grown SiO_2 gate oxide and devices after postoxidation annealing in NO showed that the annealing process had almost no effect on the intrinsic mobility. The improvement in performance was mainly attributed to increased channel carrier density. However, there has been an intense debate with regard to the source of the extra carriers. One school claims that the improvement in field-effect mobility is mostly attributed to the introduction of new positive fixed charges in the oxide by the NO annealing process [10]. This positive charge compensates the negative charge of the trapped electrons and causes a reduction in V_{TH} and an increase in the channel carrier density. Another school claims that the annealing process simply passivates the preexisting traps [11],

Manuscript received October 1, 2007; revised April 8, 2008. This work was supported in part by the National Institute of Standards and Technology (NIST) Office of Microelectronics Programs and in part by the Office of Naval Research. The review of this paper was arranged by Editor G. Pensl.

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Digital Object Identifier 10.1109/TED.2008.926626

and as a result, more electrons are free to flow in the channel. A third school considers both trap passivation and an increase in the positive fixed charge [12]. The question whether nitrogen treatment improves the field-effect mobility by passivation of the oxide traps, by adding a positive fixed charge to the oxide bulk, or by both, remains unanswered.

The drain current and threshold voltage instabilities in 4H-SiC MOSFETs under normal operating conditions are completely reversible and repeatable. There is no accumulated damage to the oxide, and it can safely be assumed that these instabilities are the result of transient charge trapping in the oxide. Therefore, passivating the oxide traps should reduce the instability. In this paper, the drain current and threshold voltage instabilities have been studied using fast I–V measurements of devices with postoxidation annealing treatment in NO environment and with no treatment. The results show that postoxidation annealing treatment with NO dramatically reduces the instability. No difference in the fixed charge density was found after the annealing treatment. Hence, for the devices tested in this paper, the improvement in the field-effect mobility is attributed to the oxide trap passivation by the annealing process.

II. Experiment

State-of-the-art 4H-SiC MOSFETs with a 50-nm-thick SiO_2 thermally grown gate oxide and a polysilicon gate electrode from two different wafers were studied. One of the wafers had a thermally grown SiO_2 oxide ("as grown"), whereas the second one had a similarly grown gate oxide with additional postoxidation annealing in NO environment. The dimensions of all the devices were 424 μm $\times$ 1 μm.

Fast measurements of the drain current were performed using a low-noise high-speed operational amplifier following the setup of Shen *et al.* [13]. Fig. 1(a) shows a schematic setup of the fast I–V measurement. In this experiment, we used two different stress patterns. The fast measurement setup enabled us to separately study the positive and negative bias stress effects. In order to study the effect of a positive bias stress, a trapezoidal stress pattern, as depicted in Fig. 1(b), was used. During the ON state of the pulse, a positive gate stress bias $V_{\rm STRESS}$ was applied for the duration of the stress interval. The I–V curves were captured during the rise and fall times of the pulse. To study the effect of a negative bias stress, we composed a special stress pattern, as depicted in Fig. 1(c). First, the gate voltage is swept up while capturing the first I–V curve. Then, the gate voltage is immediately switched to the negative stress bias. At the end of the stress interval, the gate voltage is swept back up while capturing the second I–V curve. This minimizes the time a positive bias is applied to the gate. For both cases, the stress patterns were periodically applied to the gate with a 2-s detrapping phase at 0 V between each repetition. In all the experiments, the drain bias was kept at 0.5 V. The I–V transfer characteristics were measured at up to 10 gigasamples/s, and the capture time varied from a few seconds down to 10 μs. $V_{\rm TH}$ was defined as the value of the gate bias when the drain current reaches 1 μA. The $V_{\rm TH}$ instability $\Delta V_{\rm TH}$ is defined as the difference between $V_{\rm TH}$ measured before and after the stress. The speed of the amplifier sets the limit for the fastest

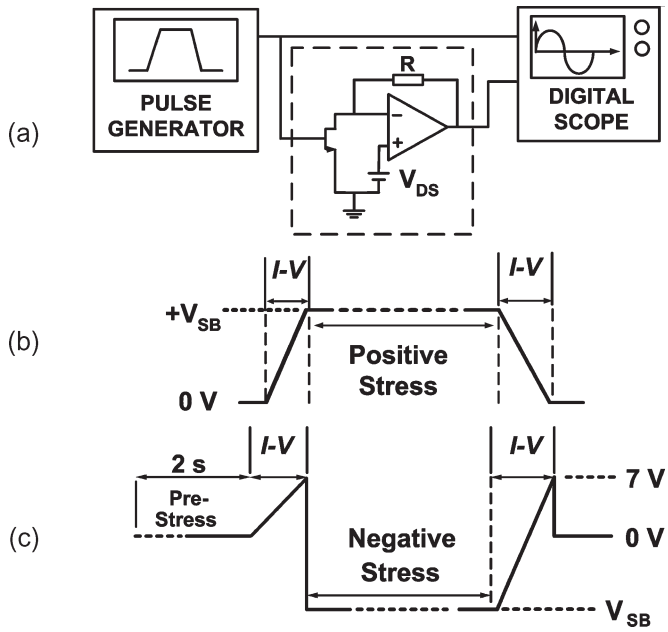

Fig. 1. (a) Schematic of the fast I–V measurement setup. (b) Positive bias stress pattern. (c) Negative bias stress pattern.

I–V measurement time to 10 μs, because even a short delay between the gate and drain signals of a few nanoseconds can cause a large shift in the I–V curve. In addition, the coaxial cables, which connect the amplifier and the pattern generator to the scope, must be kept at the same length to avoid an additional delay between the signals. The displacement current through the parasitic drain-to-gate capacitor $C_{\rm GD}$ can greatly influence the measured drain current. In order to simplify the data processing, the displacement current was kept at negligible levels ($< 1\%$ of the channel current).

To achieve faster characterization, the drain current decay ΔI_D was measured in response to an abrupt gate bias pulse. Thus, the gate and drain signals do not have to be perfectly synchronized, the measurement is only limited by the settling time of the amplifier, and more abrupt pulses with rise and fall times down to 1 μs were used. All the measurements were performed at room temperature.

III. Results and Discussion

A. Conventional DC Characterization

Initially, both types of MOSFETs were characterized by means of conventional dc measurements using a parameter analyzer. The field-effect mobility was extracted from the I–V transfer characteristics. The typical measurement time of a single I–V curve was in the range of seconds. Fig. 2(a) shows the I_D–$V_{\rm GS}$ transfer characteristics of 1- and 3-μm-long SiC MOSFETs with as-grown SiO_2 oxide and after postoxidation annealing in NO. The field-effect mobility was extracted from the I–V curves and is shown in Fig. 2(b). The devices with an as-grown SiO_2 gate oxide has a much lower field-effect mobility and a much higher threshold voltage. This poor device performance of the as-grown devices is attributed to the high density of preexisting oxide traps near and at the SiC/SiO_2 interface. The trapped charge in the oxide causes reduction

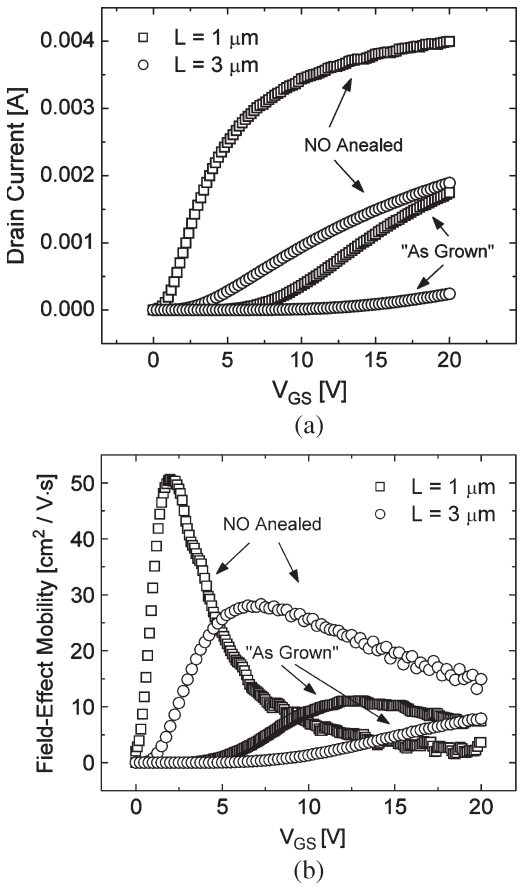

Fig. 2. (a) $I_D-V_{\rm GS}$ transfer characteristics and (b) extracted field effect mobility of (squares) 1-μm-long and (circles) 3-μm-long SiC MOSFETs with as-grown SiO_2 and after postoxidation annealing in NO environment.

in the mobile charge of the inversion layer, threshold voltage increase, and mobility degradation due to Coulomb scattering. It is worth noting that the field-effect mobility of the 1-μm-long NO-annealed device rapidly decreases with gate bias after reaching its peak and becomes even lower than the as-grown mobility at high gate biases. This rapid decrease is due to short-channel effects. For the longer channel devices (over 3 μm), the mobility of both as-grown and NO-annealed devices at very high gate biases asymptotically approaches a similar value, but the NO-annealed mobility is still twice as high as the as-grown mobility even at $V_{\rm GS} = 20$ V [see Fig. 2(b)]. The 1-μm-long devices were used for the transient characterization due to their higher current values. Thus, the displacement current through the parasitic drain-to-gate capacitance was very low and could be neglected. In addition, the signal-to-noise ratio was much better. At the same time, the transient behavior of the device is not channel length dependent, and all the results are valid for longer channel devices.

There is a disagreement between the current and the mobility results in Fig. 2. The 1-μm-long NO-annealed sample drives more than double the drain current of the as-grown sample at $V_G = 20$ V, but the mobility is much lower at $V_G = 20$ V. The difference in the threshold voltage (estimated at 6 V) is not sufficiently high to explain this discrepancy. A possible explanation is that during the conventional slow I–V measurement, carriers are being trapped in the oxide, and the threshold voltage increases. As a result, the threshold voltage difference at

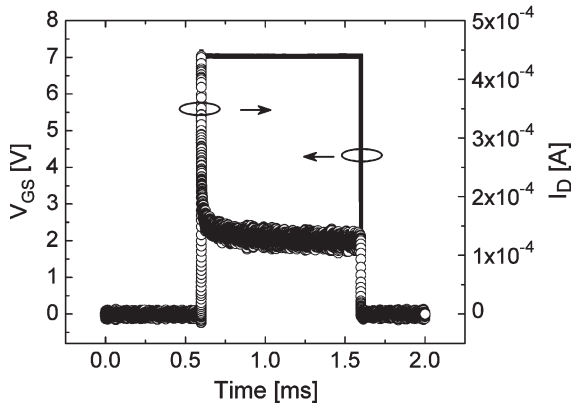

Fig. 3. (Open circles) Drain current response of a 1-μm-long SiC MOSFET with as-grown SiO_2 to a (full squares) 1-ms gate bias pulse with rise and fall times of 1 μs. The stress bias $V_{\rm STRESS}$ was 7 V.

$V_G = 20$ V is much larger than 6 V. The strong dependence of $\Delta V_{\rm TH}$ on the gate bias (see Figs. 6 and 7) and on the measurement time [Figs. 4 and (5)] supports this explanation. The field-effect mobility is extracted from dI_D/dV_G using $\mu = (C_{\rm OX} \cdot W/L \cdot V_{\rm DS})^{-1} \cdot dI_D/dV_G$. This is a differential value and is different than the mobility absolute value, particularly when $V_{\rm TH}$ is a function of V_G. Another possible explanation is that dopant diffusion during the annealing process decreases the effective channel length of the NO-annealed devices. However, this is less reasonable because a larger discrepancy was found for longer channel transistors, where the channel length differences can be neglected.

B. Transient Trapping in Devices With As-Grown SiO_2

1) Effect of the Measurement Speed: Since the time constants of these transient trapping and detrapping processes vary from milliseconds down to less than a microsecond, the full impact of this phenomenon may not be captured by conventional dc measurement techniques. Therefore, the as-grown SiO_2 devices were characterized using the fast I–V measurement setup. The drain current pulse response is shown in Fig. 3. After only 1 ms, the drain current decreases to less than 33% of its initial value. This transient behavior is totally reversible and repeatable. This suggests that the instability is due to charge trapping into preexisting traps, and there is no accumulated damage to the device.

The effect of the measurement time on the I–V transfer characteristics and on the threshold voltage and drain current instabilities, i.e., $\Delta V_{\rm TH}$ and ΔI_D, respectively, is shown in Figs. 4 and 5. Fig. 4 shows the $I_D-V_{\rm GS}$ transfer characteristics measured using a positive trapezoidal stress pulse, as depicted in Fig. 1(b), with different rise and fall times (1 μs, 10 μs, 1 ms, and dc sweep). Fig. 5 shows $\Delta V_{\rm TH}$ and ΔI_D after a positive bias stress as a function of the measurement time. It is clear that as the measurement time reduces, the instability increases.

Although the change in $\Delta V_{\rm TH}$ appears to saturate for measurement times shorter than 10 μs (see Fig. 5), ΔI_D constantly increases. The reason for this discrepancy is the limitation of the measurement instrumentation. For such short measurement times, the amplifier delay causes a slight shift to the right (rising V_G) or to the left (falling V_G) of the I–V curve. As a result, the

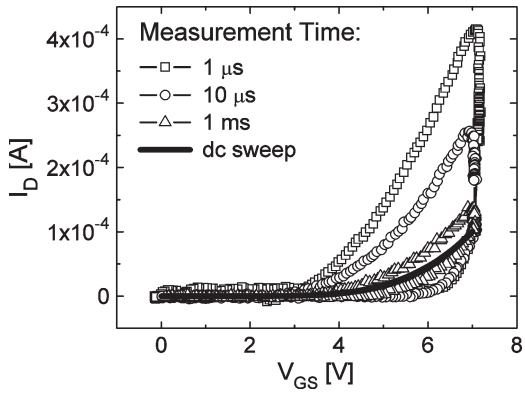

Fig. 4. $I_D-V_{\rm GS}$ transfer characteristics of a 1-μm-long SiC MOSFET with as-grown SiO_2 measured using a positive stress pulse with different rise and fall times. (Squares) 1 μs, (circles) 10 μs, (triangles) 1 ms, and (solid curve) dc sweep. The stress bias $V_{\rm STRESS}$ was 7 V, and the stress interval was 100 ms.

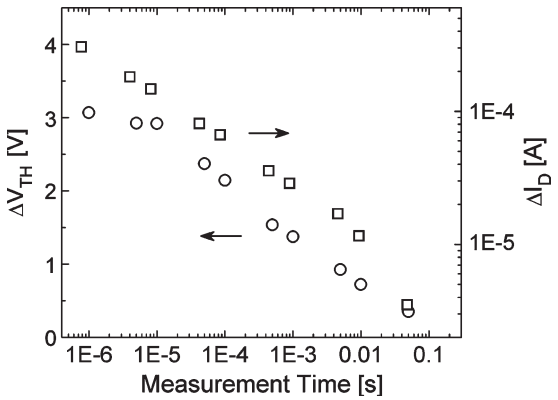

Fig. 5. (Circles) $\Delta V_{\rm TH}$ and (squares) ΔI_D of a 1-μm-long SiC MOSFET with as-grown SiO_2 after a positive bias stress as a function of the measurement time. The stress bias $V_{\rm STRESS}$ was 7 V, and the stress interval was 100 ms.

measured hysteresis is slightly smaller. Nevertheless, the 1-μs curve is included in Fig. 4 to emphasize the exponential effect of the measurement time. In contrast to $\Delta V_{\rm TH}$ extraction, ΔI_D is not affected by this delay because only a single signal I_D is considered. Therefore, faster measurement times are achievable. It is important to notice that even with a measurement time of only 1 μs, the measured instability still increases. Thus, with a faster instrumentation, even higher ΔI_D would be measured.

By switching the gate voltage in only 1 μs, the drain current is almost five times larger than that under dc conditions (see Fig. 5). Moreover, the drain current continues to increase as faster rise times are applied. These results indicate that a much higher performance can be achieved if the oxide trap density is reduced to a minimum. Additionally, fast I–V measurements are needed to decouple the effect of transient trapping and study the intrinsic properties of the SiC MOSFET channel.

2) Effect of the Stress Bias: The effect of the stress bias on $\Delta V_{\rm TH}$ and ΔI_D is shown in Figs. 6–8. Fig. 6 shows the $I_D-V_{\rm GS}$ transfer characteristics after a positive bias stress as a function of the stress bias. Fig. 7 shows $\Delta V_{\rm TH}$ and ΔI_D as a function of the stress bias. The measurement time was 20 μs, and the stress interval was 100 ms. Both ΔI_D and $\Delta V_{\rm TH}$ linearly increase with the positive stress bias. Fig. 8 shows the $I_D-V_{\rm GS}$ transfer characteristics after a negative bias stress. The

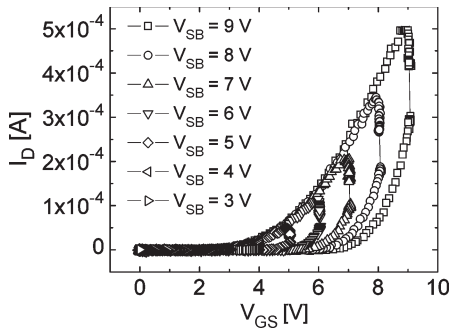

Fig. 6. $I_D-V_{\rm GS}$ transfer characteristics of a 1-μm-long SiC MOSFET with as-grown SiO_2 measured using a positive stress pulse with different stress biases $V_{\rm STRESS}$. The measurement time was 20 μs, and the stress interval was 100 ms.

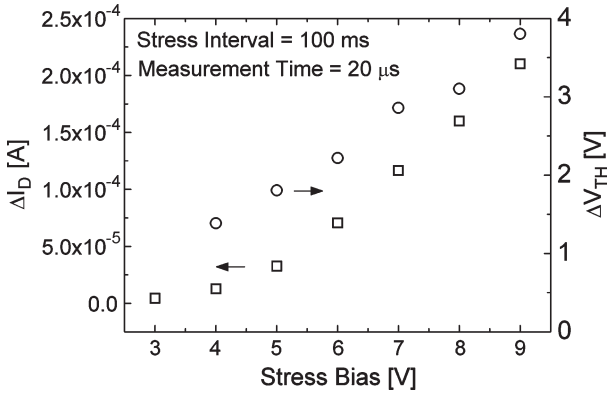

Fig. 7. (Circles) $\Delta V_{\rm TH}$ and (squares) ΔI_D of a 1-μm-long SiC MOSFET with as-grown SiO_2 as a function of the stress bias $V_{\rm STRESS}$. The measurement time was 20 μs, and the stress interval was 100 ms.

I–V curves were measured using the special stress pattern, as depicted in Fig. 1(c). In Figs. 6 and 7, it is evident that the total charge in the oxide linearly increases with the applied positive gate stress bias. On the other hand, under a negative bias, the charging effect is negligible (see Fig. 8). This result suggests that the trap energy profile is asymmetric with a large density of traps located at the upper half of the band gap.

Under a positive bias, the Fermi level is close to E_C, and the channel is inverted. Interface traps in the upper half of the band gap are negatively charged as their level falls below the Fermi level. As a result, the negative oxide charge shifts $V_{\rm TH}$ to a higher value. The applied negative bias stress was always below the flat-band voltage. Thus, the MOS structure was in accumulation, the channel was filled with holes, and the Fermi level was close to E_V. If the energy profile of the traps was symmetric, one would expect that the traps located at the lower half of the band gap were positively charged. A positive charge in the oxide shifts the threshold voltage to a lower value. However, no change in the threshold voltage was observed; hence, there were no traps in the lower half of the band gap. This asymmetric distribution of interface traps in the band gap of 4H-SiC with a high density of traps close to the conduction band edge has already been reported in the past [1], [14], [15].

3) Effect of the Stress Interval: Fig. 9 shows $\Delta V_{\rm TH}$ (triangles) and ΔI_D (squares for fast I–V and circles for

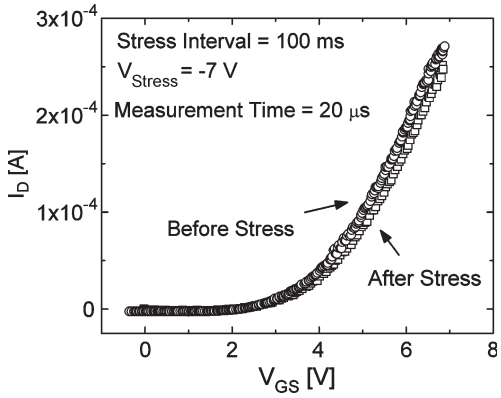

Fig. 8. $I_D-V_{\rm GS}$ transfer characteristics of a 1-μm-long SiC MOSFET with as-grown SiO_2 measured using a negative stress pattern [depicted in Fig. 1(c)] with a stress bias $V_{\rm STRESS}$ of -7 V. The measurement time was 20 μs, and the stress interval was 100 ms.

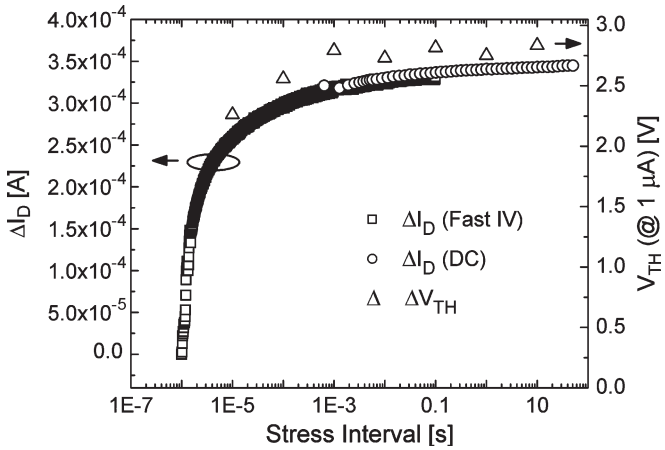

Fig. 9. (Triangles) $\Delta V_{\rm TH}$ and (squares for fast I–V and circles for conventional dc) ΔI_D of a 1-μm-long SiC MOSFET with as-grown SiO_2 as a function of the stress interval. The stress bias $V_{\rm STRESS}$ was 7 V.

conventional dc) after a positive stress as a function of the stress interval. The data points were obtained from three different experiments. In the first experiment, each $\Delta V_{\rm TH}$ data point was generated from separate uninterrupted gate pulses of different time intervals. In the second experiment, ΔI_D data points were generated from a single 100-ms gate pulse response using fast I–V measurements. In the third experiment, ΔI_D data points were generated from a single 50-s gate pulse response using conventional dc measurements (by a parameter analyzer). The superimposed data points from all three experiments give accurate time dependence over more than seven time decades.

Both $\Delta V_{\rm TH}$ and ΔI_D exhibit a complicated time dependence (see Fig. 9). Immediately after the gate bias switching, there is a rapid reduction in I_D. After about 1 ms, I_D continues to slowly decrease with a linear dependence on $\log(t)$. Recently, Potbhare *et al.* [16] have simulated the transient trapping in SiC MOSFETs using a physical model containing both shallow and deep interface traps. The simulated $I_D(t)$ is very similar to the experimental results. According to this model, the initial fast instability is due to electron trapping in interface traps that are close to E_C and have relatively short trapping time constants, whereas the subsequent slower instability is due to electron trapping in "slow" midgap interface states.

Apart from interface trap population, tunneling of carriers from the channel into bulk oxide traps is a well-established model for describing the threshold voltage instability in Si MOSFETs with radiation damage or Si MOSFETs with high-κ gate dielectrics [17], [18]. Additionally, tunneling into oxide traps has been suggested to explain the time dependence of threshold voltage instabilities in SiC MOSFETs [7], [8]. The simplest tunneling model [19] describes tunneling of electrons from the inversion layer to a single trap through a potential barrier. Since the electron wave function exponentially decays into such a barrier, the time constant associated with a trapping event exponentially increases with the distance in the oxide, i.e., $\tau = \tau_0 \exp(2\alpha \cdot x)$, where x is the distance into the oxide, and τ_0 is the fundamental transition time of the tunneling process. α is the tunneling coefficient and depends on the barrier height and the electron effective mass in the oxide. If the SiC/SiO_2 parameters are selected, a time constant of 1 s is obtained for a distance of 2.6 nm into the oxide. Electron energy loss spectroscopy (EELS) measurements have shown a carbon-rich transition layer expanding several nanometers into the oxide [2]. Therefore, the transient trapping should continue for long timescales.

The "tunneling front" model [17], which describes carrier motion in the oxide bulk via trap-assisted tunneling between bulk traps, is widely used to model threshold voltage instability in Si MOSFETs with radiation damage. This model assumes a uniform spatial distribution of bulk oxide traps and predicts a linear dependence of the instability with $\log(t)$, which is similar to the measured results at stress intervals longer than 1 ms. Another indication of the existence of bulk oxide traps was presented by Tilak *et al.* [20]. They have shown that the trapped charge in the oxide of SiC MOSFETs continues to increase with the gate bias even after the Fermi energy is within the conduction band. Hence, bulk traps have to be present in addition to the interface traps.

All of the aforementioned results suggest that both interface traps and bulk oxide traps, which are spatially distributed away from the SiC/SiO_2 interface, take part in the trapping process.

C. Comparison Between As-Grown SiO_2 and NO-Treated Devices

The measurements of the NO-annealed devices were done under similar conditions as previously mentioned. The drain current pulse response is shown in Fig. 10. In contrast to the as-grown SiO_2 devices, no change in I_D (open circles) is noticed even after 100 ms of ON pulse time.

Fig. 11 shows the $I_D-V_{\rm GS}$ transfer characteristics after a positive bias stress. Although there is no observable decay in drain current, a small shift in the I–V curve was noticed. The inset of Fig. 11 shows the magnitude of $\Delta V_{\rm TH}$ as a function of the stress interval. This shift is more than an order of magnitude lower than the as-grown SiO_2 device and has a very weak dependence on the stress interval.

The $I_D-V_{\rm GS}$ transfer characteristics after a negative bias stress are shown in Fig. 12. Similarly to the devices with as-grown SiO_2, the shift in threshold voltage and the change in I_D due to negative bias stressing are negligible.

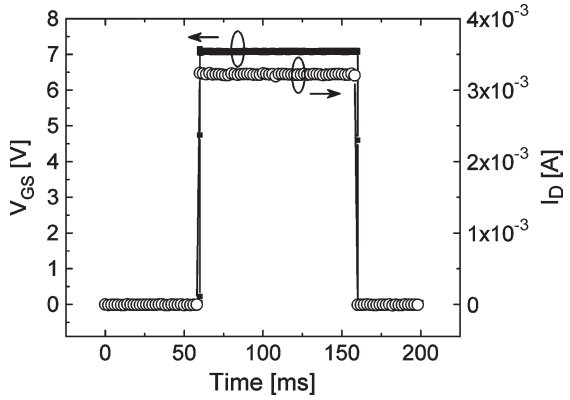

Fig. 10. (Open circles) Drain current response of a 1-μm-long SiC MOSFET with postoxidation annealing in NO environment to a (full squares) 100-ms gate bias pulse with rise and fall times of 1 μs. The stress bias V_{STRESS} was 7 V.

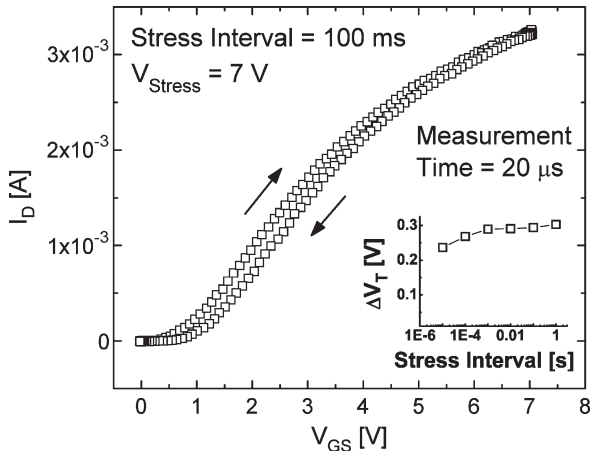

Fig. 11. I_D-V_{GS} transfer characteristics of a 1-μm-long SiC MOSFET with postoxidation annealing in NO environment taken using a positive stress pulse with a stress bias V_{STRESS} of 7 V. The measurement time was 20 μs, and the stress interval was 100 ms. Inset shows a negligible ΔV_{TH} dependence on the stress interval.

The drain current and threshold voltage instabilities under normal operating conditions are assumed to be the result of transient charge trapping in the oxide. From a comparison of the fast I–V measurement results from as-grown SiO_2 and NO-annealed devices, it is clear that postoxidation annealing in NO drastically reduces the transient trapping, thus implying a significantly reduced trap density.

Spatially resolved EELS measurements [21] show that following annealing in NO, nitrogen is exclusively incorporated within $\sim$1 nm of the SiO_2/SiC interface. This is in agreement with the carbon-rich transition layer observed in as-grown SiO_2 at the same region and was believed to be the cause of the high oxide trap density. The nitrogen atoms passivate the oxide defects in the transition layer.

This outcome correlates with the channel carrier density results obtained using Hall effect measurements. The latter revealed a much lower carrier density in as-grown devices. The fast I–V results indicate that the "missing" carriers are trapped in the gate oxide. From C–V measurements (published elsewhere [22]) of both as-grown and annealed devices, we have found no difference in the flat-band voltage and no increase of the oxide fixed charge after NO annealing. We suggest that the

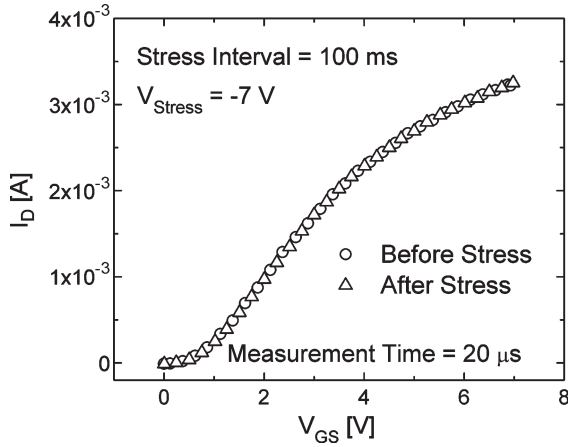

Fig. 12. I_D-V_{GS} transfer characteristics of a 1-μm-long SiC MOSFET with postoxidation annealing in NO environment measured using a negative stress pattern [depicted in Fig. 1(c)] with a stress bias V_{STRESS} of -7 V. The measurement time was 20 μs, and the stress interval was 100 ms.

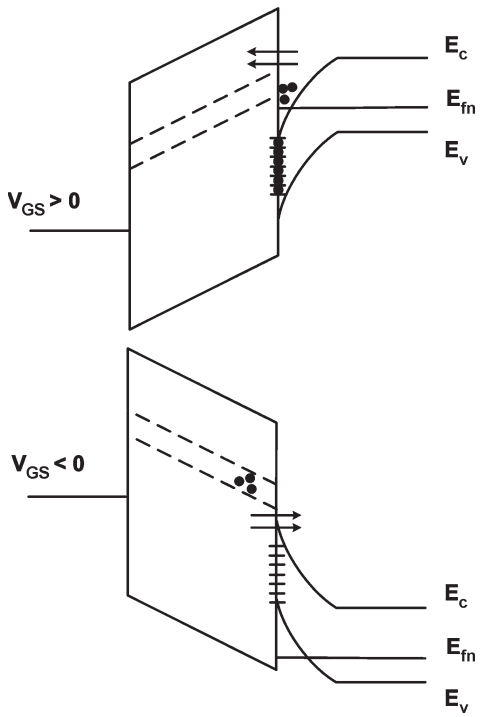

Fig. 13. Schematic energy band diagram of a SiC/SiO_2 system containing a defect band and interface traps under positive and negative gate biases.

increased positive fixed oxide charge after treatment with nitrogen is a process-related phenomenon [10], [12]. Each of the various techniques used for nitrogen incorporation, such as implantation, N_2O oxidation, and postoxidation annealing in NO environment, may affect the fixed charge density. For the tested devices in this paper, the improvement in field-effect mobility is attributed to trap passivation and not to excess fixed charge.

Although the drain current decay was negligible after the postoxidation annealing in NO, a small shift in the I–V curve is still noticed (see Fig. 11). This suggests that the annealing process does not completely eliminate the oxide traps and that further optimization is possible. Quantitative values of D_{it} and the fixed charge density of the NO-annealed devices were published elsewhere [23].

D. Physical Model

The results indicate high densities of interface and bulk oxide traps in the as-grown SiO_2 gate oxide on SiC. In addition, they show that the traps are asymmetrically distributed in energy, mostly in the upper half of the band gap [1], [14], [15]. Based on the experimental results, the following model is proposed: A defect band in the SiO_2 oxide is positioned above the SiC conduction band edge. The defect band moves on the energy scale with the gate bias, as shown in Fig. 13. In addition, interface traps are located at the SiC/SiO_2 interface and are distributed in energy throughout the band gap. As the gate bias is switched to a positive value, electrons rapidly occupy the interface traps below the Fermi level, and subsequently, the preexisting defects in the bulk of the SiO_2 are charged by tunneling. The trapped negative charge in the oxide causes reduction in the mobile charge of the inversion layer, threshold voltage increase, and mobility degradation due to Coulomb scattering. When the bias is reversed, the interface traps above the Fermi level are rapidly depopulated, and subsequently, the trapped charge in the oxide tunnels back to the SiC substrate. After the postoxidation annealing with NO, the nitrogen atoms passivate most of the oxide and interface defects and reduce the transient trapping. As a result, the channel carrier density is much higher, the threshold voltage is lower, and the field-effect mobility is higher.

IV. Conclusion

V_{TH} and I_D instabilities in state-of-the-art 4H-SiC MOSFETs have been studied using conventional dc and fast I–V measurements. The fast transient trapping and detrapping processes caused conventional dc measurement techniques to underestimate the severity of this phenomenon. These instabilities may be explained by trapping of channel electrons in preexisting traps in the bulk of the gate oxide. These traps were asymmetrically distributed in energy with a high trap density at the upper half of the band gap. Postoxidation annealing in NO passivated the traps, and as a result, the transient trapping was almost eliminated. A physical model explaining the role of the nitrogen in passivating the oxide defects was proposed.

Acknowledgment

The authors would like to thank Cree, Inc., for supplying the samples for this paper.

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