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Study of leakage-induced photon emission processes in sub-90 nm CMOS devices

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Abstract

Sub-90 nm n-MOSFETs have been studied at the sub-threshold and saturation operating regimes using infra-red photon emission intensity and current measurements. The results show a distinctive difference in the photon emission yield profile below and above threshold. A new mechanism for the higher photon emission rates in the sub-threshold regime is proposed. Electrical measurements together with 2-D numerical device simulations were carried out in order to verify this new mechanism.

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Keywords: MOSFET; Hot carrier luminescence; Photon emission; Substrate current; Leakage current; Sub-threshold current

1. Introduction

As threshold voltage, channel length and gate oxide thickness of deep sub-micron CMOS circuits are reduced, the leakage current is becoming a significant contributing factor to the total power dissipation. As a result of this down scaling, leakage current-induced photon emission increases dramatically.

Among the different leakage mechanisms [1], three major contributors are considered: sub-threshold weak inversion leakage, gate-oxide tunneling leakage, and reverse-bias drain–substrate and source–substrate junction band to band tunneling (BTBT) leakage. Other leakage components, such as gate-induced-drain–leakage (GIDL) and punchthrough current are usually ignored under normal operation conditions [2]. Each of the leakage components is strongly dependent on device geometry, doping profile, and temperature. The threshold voltage down scaling and its reduction due to short channel effects (SCEs), (e.g., drain-induced-barrier-lowering (DIBL) and roll-off) result in exponential increase of the sub-threshold current. The aggressive scaling of the oxide thickness results in high direct tunneling currents through the gate insulator of the transistor. The high-doping density near the source–substrate and drain–substrate junctions causes significantly large BTBT currents through these junctions under high reverse bias conditions.

Several models have been proposed to describe the mechanism behind the optical emission from saturated MOSFETs. Of special interest is hot-carrier emission by intra-band transitions and bremsstrahlung [3]. This model was further refined by Villa et al. [4] and it is regarded as the major cause of photon emission by hot carriers. The emission from the off-state MOSFET started to be noticeable in devices from the 180 nm technology [5] and increases dramatically for shorter gate lengths. Although the emission mechanism is not clear [6], the rapid develop-

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ment of infrared detectors in recent years allowed relatively easy registration of the faint emission and its application for integrated circuits debugging [5,7]. Polonsky et al. [6] managed to show correlation between device electrical parameters and the sub-threshold emission intensity. Each one of the leakage mechanisms described above is expected to give rise to photon emission in the sub-threshold regime.

The purpose of this study is to investigate the physical and electrical parameters that control the off-state emission intensity for deep sub-micron processes and to examine whether the emission in the sub-threshold regime could be correlated with the familiar hot carrier thermalization processes known from saturated MOSFETs.

2. Experimental details

Infrared photon emission and electrical measurements were taken on test devices manufactured using a 90 nm advanced microprocessor technology [8]. The devices used for measurements were n-MOSFETs with an effective gate length of 80 nm and a width of 9.69 μm. *I–V* characteristics and substrate currents were measured using a semiconductor parameter analyzer model HP4155B. The device emission characteristics were evaluated using a cryogenically cooled MgCdTe focal plane array IR microscope with spectral response ranging between 800 nm and 1500 nm. The total emission intensity was integrated over the entire spectral response of the detector and summed, after subtraction of background signal, for all pixel values that correspond to the transistor region.

3. Results

3.1. Photon emission intensity and substrate current

The substrate current (I_B) at the above-threshold regime was historically correlated with the hot carrier optical emission rate (N_{PH}) from MOSFETs. N_{PH} is defined as the number of photons emitted from a device per second. N_{PH} is the product of the electron current and the photon emission probability (photon yield).

Photon emission rate and the substrate current in the above-threshold regime were found to be empirically related [8] to the high electric field in the "pinch-off" region near the drain according to:

$$N_{PH} = I_{DS} \cdot \alpha_{PH} \propto I_{DS} \cdot E_{Max} \cdot \exp\left(-\frac{B_{PH}}{E_{Max}}\right) \quad (1)$$

where I_{DS} is the channel current α_{PH} is the photon yield and B_{PH} is the photon emission coefficient. E_{Max} is the maximum lateral electric field in the channel and it is modeled as:

$$E_{Max} = [V_{DS} - V_{DSAT}(V_{GS})]/\ell_D \quad (2)$$

where V_{DSAT} is the drain saturation voltage and ℓ_D is the characteristic length of the velocity saturation region. Fig. 1 shows the photon emission intensity normalized to its maximum value together with the substrate current, both measured as a function of V_{GS} at $V_{DS} = 1.3$ V. The extension of the measurement to the sub-threshold regime indicates that the substrate current does not follow the photon emission in that regime.

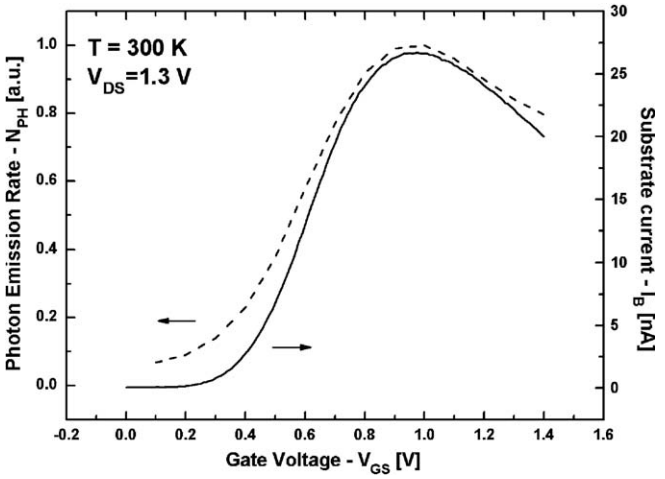

Fig. 1. Photon emission rate (dashed curve) and substrate current (solid curve) as a function of gate bias at $V_{DS} = 1.3$ V.

According to Eq. (1), the N_{PH}/I_{DS} ratio represents the photon emission yield. The impact ionization yield can be represented in a similar manner, I_B/I_{DS}. Fig. 2(a) and (b) show the measured photon emission rate and the substrate current normalized to the channel current as a function of V_{GS} at two different fixed V_{DS} values. The gate voltage is swept from the sub-threshold ($V_{GS} < 0.3$ V) to the above-threshold values ($V_{GS} > 0.3$ V).

These curves demonstrate different photon emission yield slopes at the sub-threshold and above-threshold. The distinctive behavior of the two regions may indicate that two different processes are involved in the sub-threshold and above-threshold regimes [6].

4. Discussion

It is evident from Fig. 2(a) and (b) that the photon emission and the substrate current yields as a function of V_{GS} have a much larger slope below threshold. This difference could be attributed to an additional generation mechanism active in the sub-threshold regime. Polonsky et al. [5] has suggested that the deficient emission yield at the above threshold is attributed to higher surface scattering at stronger normal electrical field.

We propose a new mechanism for the higher photon emission yields in the sub-threshold regime. The negative gate–drain bias effectively forms an accumulation layer at the silicon surface under the gate. Due to the presence of accumulated holes at the surface, the surface behaves as a p-region more heavily doped than the substrate. This causes the depletion layer at the surface to be much narrower than elsewhere. The narrowing of the depletion layer at or near the surface strengthens the electric field locally,

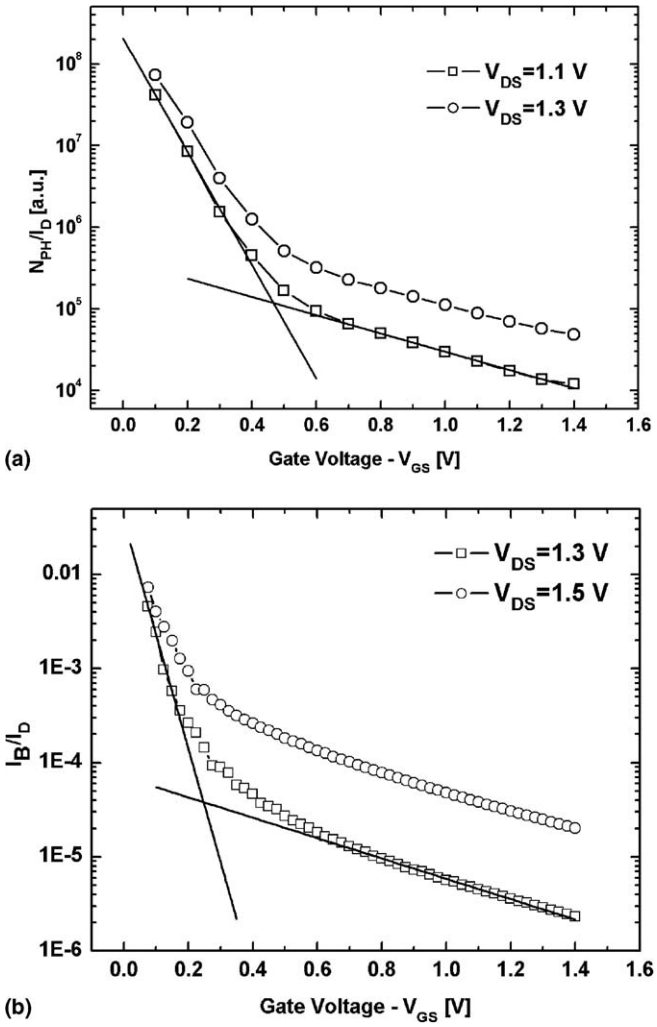

Fig. 2. Photon emission yield (a) and the substrate current yield (b), measured as a function of V_{GS} at two different fixed V_{DS} values ($V_{DS} = 1.1$ V, □; $V_{DS} = 1.3$ V, ○). Solid lines are exponential fitting.

thereby enhancing the high field effects, such as photon emission, near that region. Thus, we conclude that the electric field for sub-threshold V_{GS} cannot be represented by Eq. (2) anymore.

Numerical simulations were carried out using MINIMOS, a two-dimensional device simulator on an 0.1 μm effective channel length NMOSFET. Fig. 3 shows the simulated lateral electric field in the channel for several V_{GS} values. The electric field spatial distribution at the sub-threshold is strengthened by additional field component at low V_{GS} values attributed to the gate–drain overlapping region. Fig. 4 shows the maximum lateral electric field at the drain interface as a function of the gate voltage (open circles – simulated values, solid lines – linear fitting.). There is a clear difference in the electric field bias dependence below and above-threshold. This electric field dependence on the transistor bias conditions clearly resembles the observed photon emission yield shown in Fig. 2(a). This correlation suggests that the enhanced photon emission and substrate current yields in the sub-threshold regime

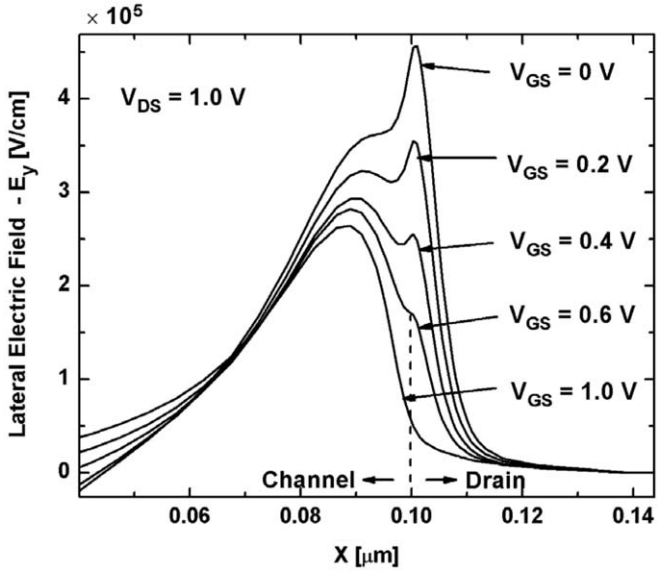

Fig. 3. Simulated lateral electric field as a function of distance along the channel for five different V_{GS} values ($V_{DS} = 1$ V). Drain mask edge is marked by the dashed line. The gate–drain overlap is 5 nm.

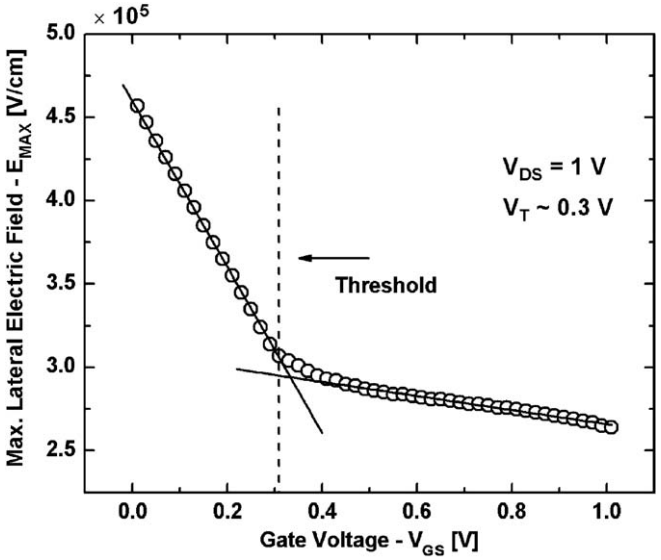

Fig. 4. Simulated maximum lateral electric field (○) at the drain edge as a function of gate voltage. $L_{mask} = 0.1$ μm. Dashed line represents the threshold voltage level.

are both attributed to this gate-induced excess electric field at the drain edge.

There are several known contributors to the off-state leakage current. However, the major contributor in 90 nm devices [1] is still the sub-threshold diffusion current. We believe that the electrons of this leakage current component, which flow from the source to the drain, are subject to the enhanced electric field near the drain, as shown in Fig. 3, and thus generate photon emission via intra-band transitions.

There may be several other plausible mechanisms that generate the additional emission: (i) intra-band transitions

during the acceleration of charge at the n/p interface due to BTBT; (ii) trap assisted recombination of charge at the n/p interface; (iii) trap assisted recombination of charges of gate induced drain leakage (GIDL) at the drain end; (iv) trap assisted recombination of diffused charge under the channel. All these obvious candidates have extremely low photon efficiency [4].

In order to verify that the additional emission is neither due to BTBT nor GIDL trap-assisted-tunneling (TAT), we measured the emission using the experimental setup from [9]. We were able to separate the effects of the vertical and lateral electric field and measure only the GIDL/BTBT component of the drain leakage photon emission. Only negligible photon emission was detected by this setup in the absence of a lateral electric field. This result indicates that the channel electrons from the sub-threshold diffusion current are responsible for the photon emission. Although the large vertical electric field due to high drain-to-gate bias enhances the photon emission, the latter does not originate from the field induced BTBT and TAT.

4.1. Temperature dependence

We studied the temperature effect on the photon emission rate. Fig. 5 shows the photon emission yield, measured as a function of V_{DS} at the sub-threshold regime ($V_{GS} = 0$ V) and in saturation ($V_{GS} = 1$ V) for two different temperatures (318 K – □, 363 K – ○). The temperature is known to have small effect on the photon emission yield above threshold [8] as easily noticed in Fig. 5. Our results show that this trend of temperature independence continues in the sub-threshold regime.

The drain leakage current comprises of several components, each of which has different temperature dependence. The total leakage current is dominated by source-to-drain carrier diffusion that increases exponentially with temperature. Since the tunneling probability of an electron through a potential barrier does not directly depend on the temperature, the gate and the junction BTBT is expected to be less sensitive to temperature variations. Saibal et al. [1] showed the effect of temperature variation for the individual leakage components of 25-nm NMOS device based on the device simulation. Their simulations show that the sub-threshold diffusion leakage current increases exponentially with temperature, the junction BTBT increases slowly with temperature and the gate leakage is almost independent of temperature.

By raising the temperature, the weight of the sub-threshold diffusion current component increases even more. If the photon emission originates from one of the other components, the N_{PH}/I_{DS} ratio is expected to change with temperature. The observed temperature independence of N_{PH}/I_{DS} clearly indicates that the photon generation depends only on the sub-threshold diffusion leakage current.

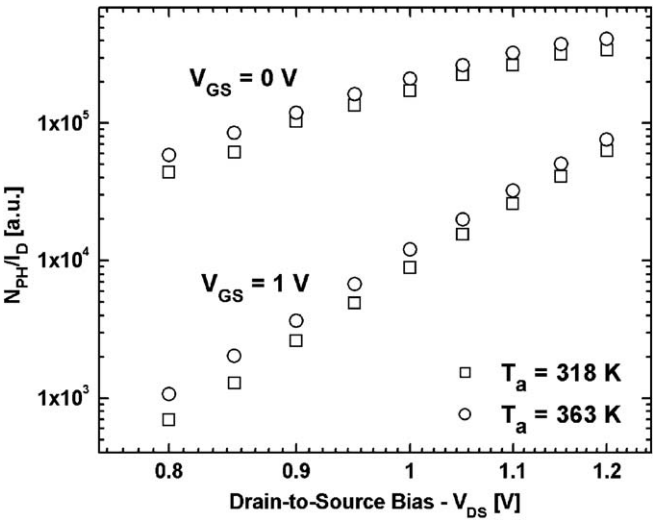

Fig. 5. Photon emission yield as a function of V_{DS} measured at two constant gate voltages $V_{GS} = 0$ V (off-state) and $V_{GS} = 1$ V (saturation), for two temperatures. □, $T = 318$ K; ○, $T = 383$ K.

5. Conclusions

Infra-red photon emission intensity and current measurements of sub-90-nm n-MOSFETs at the sub-threshold and saturation operating regimes show distinctively different V_{GS} dependence below and above the threshold voltage. The photon emission and the substrate current yields as a function of V_{GS} were found to have a much larger slope below threshold. A new mechanism for the higher slope at the sub-threshold regime is proposed. Narrowing of the depletion layer at or near the drain–gate surface locally enhances the electric field at that region. The electrons of the sub-threshold diffusion current are ''heated'' in this enhanced field and induce photon emission. Numerical simulations of the near-drain electric field and temperature resolved measurements support this model. BTBT and TAT were ruled out as possible origins of the observed photon emission.

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