Ion implantation and SiC transistor performance

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SiC metal oxide semiconductor field effect transistors grown on low-doped epilayer channels and on ion-implanted channels with either "as grown" or NO annealed thermal oxides have been electrically characterized. The threshold voltage, effective electron mobility, as well as fixed charge, oxide trap, and interface trap concentrations have been separately obtained using conventional dc sweep, capacitance-voltage (*C-V*), fast current-voltage (*I-V*), and low frequency noise measurements. The results show that devices with as grown SiO_2 have a much higher density of "slow" bulk oxide traps than devices after postoxidation annealing in NO. The oxide fixed charge density is unaffected by the annealing process. Devices fabricated on ion-implanted channels exhibit only a small increase in the slow bulk oxide trap density and the fixed charge. However, the density of the "fast" interface traps increases dramatically. This suggests that the damage due to the ion-implantation process is mainly interfacial. In contrast to Si devices, this ion-implantation damage is not completely repaired even after annealing. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3110071]

I. INTRODUCTION

The superior qualities of 4*H*-SiC have made it a prime semiconductor for high power, high voltage, and high temperature electronics. However, unacceptably low electron mobility in the channel prevents effective commercial production of SiC power metal oxide semiconductor field effect transistors (MOSFETs). The poor mobility is due to traps located in the bulk of the oxide and at the SiO_2/SiC interface. These traps reduce the mobile carrier density and increase carrier scattering. It has been found that incorporating nitrogen into the gate oxide by means of postoxidation annealing in NO or N_2O,[1,2] as well as oxidation of SiC after nitrogen ion implantation,[3] reduces the oxide trap density by orders of magnitude and consequently increases the effective mobility.

Unfortunately, the reduction in the trapped oxide charge creates a critical problem. The threshold voltage depends on the balance between the positive fixed charges and the negative trapped charge. Thus, passivating the oxide traps undermines that balance yielding a lower threshold voltage, which is undesirable for power devices. Therefore, developing a high-performance SiC MOSFET requires minimization of both the oxide trap and fixed charge densities.

The vast majority of studies conducted on SiC MOSFETs have used low-doped epitaxially grown channels. However, in commercial SiC devices the gate oxide is grown on highly doped ion-implanted *p*-wells. To date, the effect of the implantation process on the trap distribution in the device is not fully understood.

The quality of the SiO_2/SiC interface is significantly lower when the oxide is grown on ion-implanted material. The field-effect mobility reported for ion implanted devices is highly dependent on the doping concentration and is usually an order of magnitude lower than the epilayer values.[4–6] Time dependent dielectric breakdown is also more severe for implanted channel devices and shorter failure times have been reported.[7,8] The lower quality is attributed to increased scattering due to higher *p*-type doping, increased surface roughness, and possible implantation damage.[4] Recently, Agarwal and Haney[9] suggested that the implantation process may generate traps in the bulk of the SiC immediately below the SiC/SiO_2 interface. We have studied the effect of ion implantation on the physical parameters of the SiC/SiO_2 system (i.e., threshold voltage, effective electron mobility, as well as fixed charge, oxide trap, and interface trap concentrations).

II. EXPERIMENTAL SETUP

State-of-the-art 4*H*-SiC *n*-MOSFETs with 50 nm thick SiO_2 thermally grown gate oxides and polysilicon gate electrodes have been studied. Four types of MOSFETs were examined in this study. One group of MOSFETs (denoted by EPI) had an epitaxially grown channel while the second group (denoted by IMP) had an implanted channel. Both groups included devices with thermally grown SiO_2 oxide (this "as grown" group is denoted by AG) and devices with similarly grown gate oxide that underwent additional postoxidation annealing in a NO environment (denoted by NO).

The concentrations of fixed charges, oxide traps, and interface traps in each of the MOSFET types have been separately obtained using conventional dc sweep, *C-V*, fast *I-V*, and low frequency noise (LFN) measurements. dc sweep *I-V*

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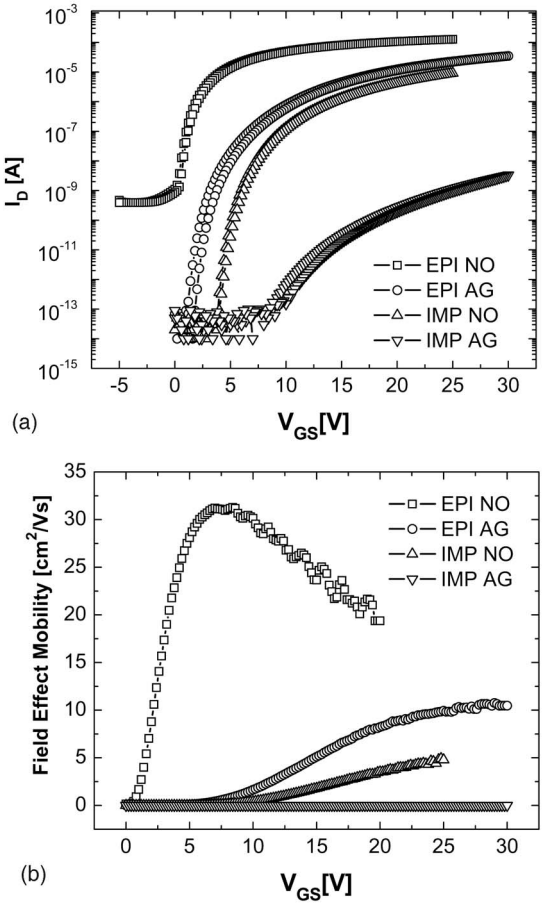

FIG. 1. (a) I_D-V_{GS} characteristics and (b) extracted field effect mobility of SiC MOSFETs of the four wafer types.

and *C-V* measurements were done with a semiconductor parameter analyzer and a *LCR* meter, respectively. Fast measurements of the drain current were performed using a low noise, high speed operational amplifier.[2] LFN measurements were performed using a standard noise measurement setup including two channel low noise dc biasing sources, a low noise voltage preamplifier, and a dynamic signal analyzer.[10]

III. RESULTS AND DISCUSSION

Figure 1(a) shows the I_D-V_{GS} characteristics of SiC MOSFETs of the four device types. The threshold voltages were extracted from the *I-V* characteristics by extrapolation in the linear regime method and are summarized in Table I. The extracted field effect mobility curves are shown in Fig. 1(b). The results show that V_{th} in IMP devices is significantly higher than EPI devices. Furthermore, V_{th} in AG devices is significantly higher than in NO devices. The close correlation between the threshold voltage and the field effect mobility indicates that the dominant parameter dictating the field effect mobility and, consequently, V_{th} of these devices is the density of mobile charge carriers in the channel. This correlates with Hall effect mobility measurements, which demonstrate almost no effect on the intrinsic mobility following NO annealing or ion implantation. The improvement in performance is attributed to oxide trap passivation and increased channel carrier density.[11]

TABLE I. Summary of the extracted threshold voltage, peak effective mobility, and flatband voltage of the different devices.

Wafer	V_{th} (V)	μ_{peak} (cm^2/V s)	V_{FB} (V)
EPI-NO	2.94	31.3	−4.8
EPI-AG	15.4	10.7	−4.8
IMP-NO	15.5	4.9	−7.8
IMP-AG	24	0.0026	−7.8

The MOSFET threshold voltage is given by

$$V_{th} = V_{FB} - 2\Phi_F + \frac{(4q\varepsilon_{SiC}N_A^-)^{1/2}}{C_{ox}}, \quad (1)$$

where V_{FB} is the flatband voltage, Φ_F is the bulk potential, q is the electron charge, ε_{SiC} is the SiC dielectric constant, N_{A-} is the ionized acceptor concentration, and C_{ox} is the oxide capacitance. The flatband voltage is generally given by

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}}{C_{ox}}, \quad (2)$$

where Q_f is the oxide fixed charge, Q_{ot} is the oxide trap charge, and Q_{it} is the interface trap charge. The contribution of each of these four parameters Q_f, Q_{ot}, Q_{it}, and N_A needs to be determined to explain the considerable difference in V_{th} between the four device types.

The two ion-implanted wafers have an order of magnitude higher doping level (1×10^{16} cm^{-3} in the IMP wafers versus 1×10^{15} cm^{-3} in the EPI wafers). Using Eqs. (1) and (2) we calculate that due to the higher doping in the IMP devices, their V_{th} increased by 0.8 V. This shift is more than one order of magnitude smaller than the observed differences and clearly cannot account for large differences in threshold values between the devices.

To determine the effect of the fixed charge, we extracted the flatband voltage from the *C-V* characteristics. Under flatband conditions, the Fermi level is close to the valence band maximum (for *p*-type substrates) so one can safely assume that all traps are empty of electrons. This does not necessarily mean that all traps are not charged (positively). However, it has been shown that the interface and bulk traps of SiC are acceptorlike and concentrated at the upper half of the band gap.[12] Thus, all the states above Fermi level should be electrically neutral. Therefore, the change in the extracted flatband voltage is attributed to the fixed charge and N_A only. It should be noted that this analysis is not valid for conventional Si/SiO_2 metal-oxide-semiconductor (MOS) devices, where the oxide traps are symmetrically distributed throughout the band gap and both acceptorlike and donorlike traps exist. Figure 2 shows the capacitance-voltage characteristics of 200×200 μm^2 SiC MOS capacitors from the four wafers. The extracted flatband voltages are summarized in Table I. The results show no change in flatband voltage between the AG oxide devices and the NO devices. This implies that the NO annealing process does not create additional fixed charge. In contrast, the flatband voltage of the IMP devices is 3 V lower than the EPI devices. After subtracting the N_A contribution, the fixed charge contribution to the V_{th} change

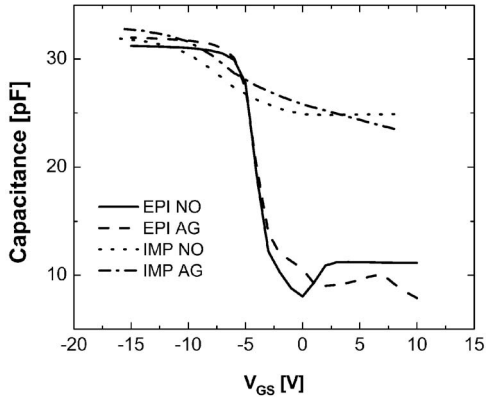

FIG. 2. Capacitance-voltage characteristics of 200×200 μm^2 SiC MOS capacitors of the four wafer types.

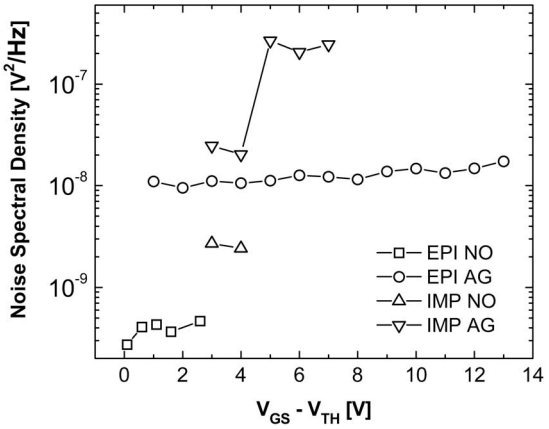

FIG. 4. Noise power spectral density at $f=30$ Hz as a function of V_G-V_{th} from the four types of MOSFETs.

in the IMP devices is -2.2 V. After considering both the contribution of the fixed charge and the different doping concentrations, they are too small to account for the large V_{th} shifts between the four types of wafers. Thus, only the trapped charge in the bulk and at the oxide interface can explain these V_{th} shifts.

The pulse response measurement enables separation between the contributions of "fast" and "slow" traps. Since the response time of a trap depends exponentially on its distance from the channel,[10] this is a good qualitative criterion for distinguishing between the contribution of interface and bulk traps. The fast interface traps are occupied faster than the rise time of the pulse and the charge trapping that takes effect during the "on" time of the pulse is attributed only to the "slow traps" in the oxide bulk. The steady-state current $I_D(t\rightarrow\infty)$ depends on the total density of traps at the interface and in the bulk of the oxide. The ratio between $I_D(t=0)$ and the steady-state value represents the ratio of the slow and fast traps or interface and bulk oxide traps. The greater the difference between $I_D(t=0)$ and $I_D(t\rightarrow\infty)$, the higher is the portion of the oxide bulk traps.[13]

Figure 3 shows the drain current pulse response of the four types of MOSFETs. The rise and fall time of the gate pulse were 1 μs. The drain current was captured using a fast

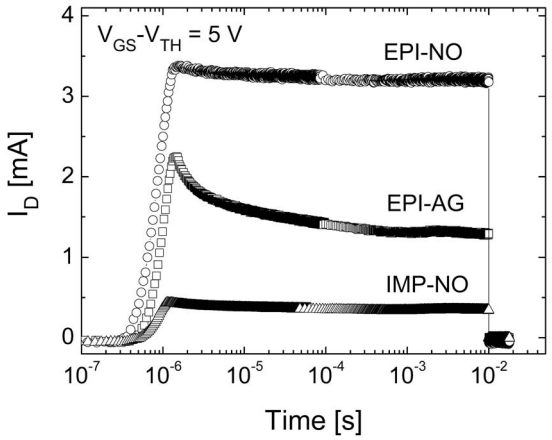

FIG. 3. Drain current pulse response of the four types of MOSFETs. The rise and fall time of the gate pulse were 1 μs. The pulse bias was normalized to the device V_{th}(V_{GS}-V_{th}=5 V).

measurement setup.[2] To have a fair comparison between the four types of devices, the pulse bias was normalized to the device V_{th}. From the steady-state current $I_D(t\rightarrow\infty)$ of the four device types in Fig. 3, it is implied that IMP devices have a higher total trap density than EPI devices. The EPI-NO device has the lowest overall trap density, followed by the EPI-AG and the IMP-NO devices. The IMP-AG device had extremely low current levels and could not be properly measured by our fast-*IV* equipment.

The $I_D(t=0)/I_D(t\rightarrow\infty)$ ratios from Fig. 3 provide additional information on the spatial distribution of the traps. $I_D(t=0)/I_D(t\rightarrow\infty)$, which is closely correlated with the slow bulk trap concentration, is much lower for NO than for AG devices. This is true for both EPI and the IMP devices. Hence, we conclude that the ion implantation has almost no effect on the slow bulk trap density and it is dictated by the annealing process. A similar trend is seen in the conventional dc I_D-V_G characteristics in Fig. 1. The NO devices exhibit only a negligible hysteretic behavior, which indicates a very low slow bulk trap density, while the AG devices exhibit a much stronger hysteretic behavior and a high density of slow (bulk oxide) traps. Thus, the large difference in the total (both bulk and interfacial) trap density and consequently in V_{th} between the IMP devices and the EPI devices may be attributed to high densities of interfacial defects due to implantation process.

LFN of the drain current is an excellent monitor for bulk oxide trap density.[14] It arises from trapping and detrapping of carriers in oxide traps. Only slow traps that are located deep in the bulk of the oxide and close to Fermi energy contribute to the noise signal. Figure 4 shows noise power spectral density at $f=30$ Hz as a function of V_G-V_{th} from the four types of MOSFETs. Similar to the pulse response and dc I_D-V_G characteristics, the LFN results indicate that AG devices have a much higher density of slow bulk traps than NO devices.

If the four types of wafer are ranked according to their trap density levels extracted from LFN and $I_D(t\rightarrow\infty)$, a prominent difference emerges. The IMP-NO device exhibits lower bulk trap densities (LFN level) than the EPI-AG device, even though its total density of traps [$I_D(t\rightarrow\infty)$ level] is

clearly higher. This result also points out that the implantation induced damage is mainly interfacial and leads to higher interface trap densities.

Distinguishing between interface and bulk traps according to their time constant is widely used for Si devices. However, the main physical assumption behind this is that the semiconductor bulk is free of traps. Recently, Agarwal and Haney[9] suggested that the implantation process may generate traps in the bulk of the SiC immediately below the SiC/SiO_2 interface. Shallow traps in the SiC bulk have extremely fast time response and our techniques cannot distinguish between traps at the SiO_2/SiC interface and shallow traps in the SiC bulk. Therefore, our results support Agarwal's speculation and indicate an unrecoverable implantation damage at the SiO_2/SiC interface in the SiC bulk or both.

IV. CONCLUSIONS

The results show that devices with as grown SiO_2 have a much higher density of bulk oxide traps than devices after postoxidation annealing in NO environment. The oxide fixed charge density is clearly unaffected by the annealing process. Devices fabricated with ion-implanted channels exhibit only a small increase in the bulk oxide trap density and the fixed charge. However, the density of the interface traps increases dramatically. This suggests that the damage due to the ion-implantation process is mainly interfacial. In contrast to Si devices, this ion-implantation damage is not completely repaired even after annealing.

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