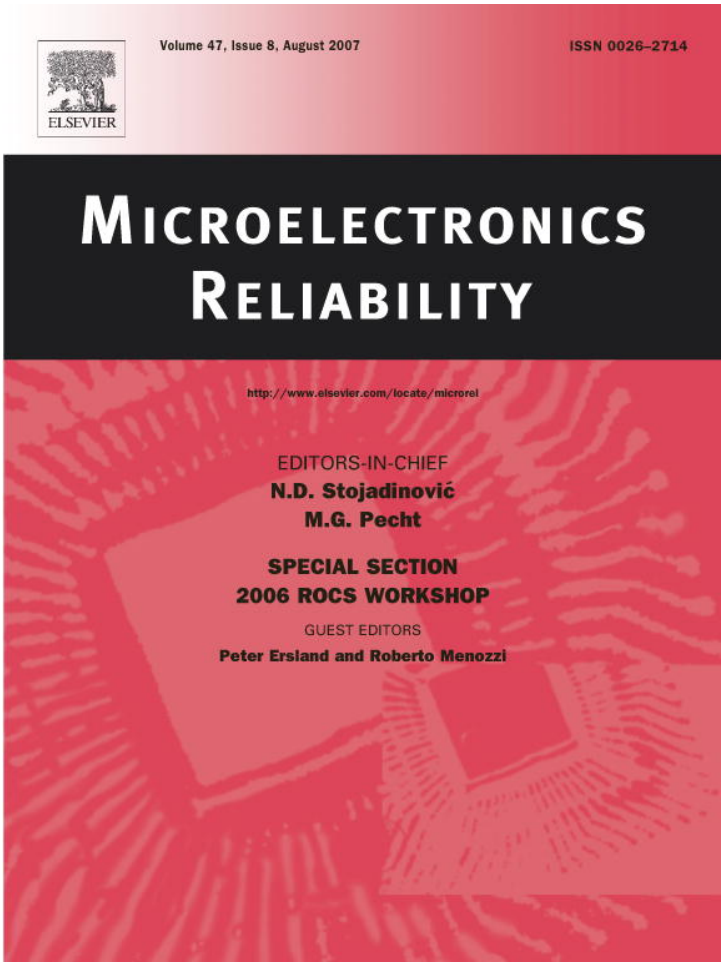

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Correlating gate sinking and electrical performance of pseudomorphic high electron mobility transistors

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Abstract

Ti interdiffusion from the Ti/Pt/Au gate into the AlGaAs Schottky barrier layer (SBL) of 0.25-μm GaAs Pseudomorphic High Electron Mobility Transistors (PHEMTs) has been studied using the accelerated life testing technique. Based on measurements and modeling, analytical expressions for quantitative correlation between the positive pinch-off voltage (V_P) shift as well as the saturation drain current (I_{Dsat}) decrease and the physical damage occurring during gate sinking has been developed. It is suggested that the main cause for device failure is the growth of the TiAs phase leading to the decrease in the SBL thickness. Additionally, it is suggested that V_P may be used as a better indicator for device degradation than I_{Dsat} since it is linearly proportional to the degrading physical characteristic – the Schottky barrier layer thickness.

1. Introduction

GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) devices are used in military and space applications, both having stringent reliability requirements. Much research has been carried out over the years, identifying various degradation mechanisms caused by thermal and electrical stressing during device operation. Gate degradation has been reported by several leading PHEMT manufacturers as a major reliability concern even under normal operation conditions. The diffusion of the gate metal into the AlGaAs SBL, i.e., the gate sinking mechanism, has been stated as the most severe cause of gate contact failure.

The gate sinking mechanism, first identified by Canali et al. [1] for GaAs MESFET devices, denotes the interdiffusion of the gate metal into the AlGaAs SBL, subsequently reducing its thickness. Since, this mechanism has been experimentally identified in PHEMT devices with different gate metals [2]. Despite immense research, gate sinking continues to be an unresolved problem as it is an inherent property of the device material, limiting device life expectancy. Modern devices use standard Ti/Pt/Au gates, due to their good Schottky contact with GaAs, having a barrier height of about 0.7–0.8 eV.

Recently, scanning transmission electron microscopy imaging has revealed physical evidence of the Ti diffusion into the AlGaAs SBL during accelerated life testing [3]. Ti diffusion into GaAs layers has been identified previously with the subsequent growth of the TiAs intermetallic phase for Ti evaporated on GaAs [4] and for Ti/Pt/Au Schottky contacts [5,6]. The newly formed TiAs phase has been found to cause a slight, though stable, shift in Schottky barrier height (0.82–0.86 eV) [7,8].

Chemical analysis using X-ray photoemission spectroscopy shows binding energy shifts for both Ga and As during annealing of Ti evaporated on GaAs. The energy shift of Ga is gradual and associated with Ti_xGa_{1-x} compound formation [9], whereas for As, a single shift is observed, caused by TiAs formation. This process is better understood by examining the isothermal section at 25 °C of the Ga–As–Ti ternary phase diagram presented in Fig. 1 [10].

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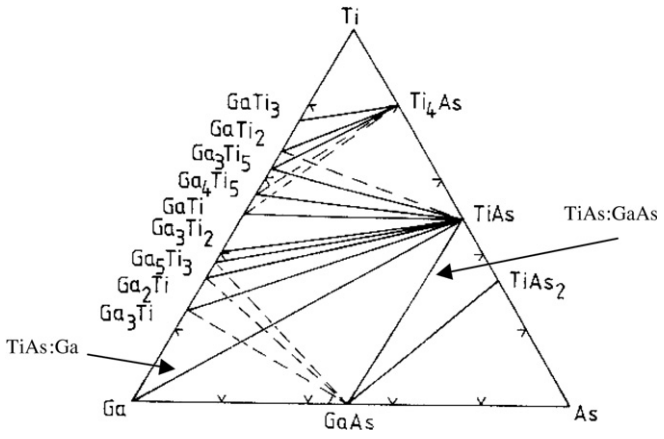

Fig. 1. The isothermal section of the Ga–As–Ti ternary phase diagram at 25 ° C (valid up to 300 °C, adapted from Ref. [10]).

It shows that the TiAs phase forms at any concentration of Ti in GaAs, leading to the expulsion of Ga from the newly formed phase. Ti has a greater affinity to As than Ga, leading to the formation of the TiAs phase with the intrusion of Ti in the GaAs. Thus, it is understood that TiAs formation is diffusion-controlled, as shown experimentally [4,6]. This is also understood from the tie lines between TiAs–GaAs and TiAs–Ga. With the introduction of Ti into the system, Ti replaces Ga, leading to the formation of TiAs:GaAs phases and causing Ga outdiffusion. Thus, after annealing Ti/GaAs samples, a layered Ti/Ti_xGa_{1-x}/TiAs:GaAs structure is expected as observed by Lee et al. [11] using transmission electron microscopy.

The TiAs growth rate has been shown to follow a parabolic rate law, given in Eq. (1), for several nanometers of Ti diffusion [4].

$$W_{\mathrm{TiAs}}^2 = D_{\mathrm{Ti}}t = D_0 t \exp\left(-\frac{E_a}{kT}\right) \quad (1)$$

where W_{TiAs} is the TiAs thickness, t is time, D_0 and E_a are the diffusion coefficient and activation energy for Ti diffusion into GaAs, respectively, k is the Boltzmann constant and T is the temperature.

The activation energy of the device degradation measured under accelerated life testing is typically in the range of 1.7 ± 0.05 eV, [3,12] for devices tested under no or low gate and drain biases, i.e., before initiating impact ionization. This value is close to the activation energy reported for Ti interdiffusion in GaAs for of Ti/GaAs samples [4,11]. This supports the assumption that Ti interdiffusion is the cause for device failure.

Several electrical parameters are known to degrade during accelerated life testing and are associated with gate sinking. The saturation drain current – I_{Dsat} has been found to decrease during the annealing process, [12,13] accompanied by a shift in the pinch-off voltage – V_{P}, to a less negative value [3]. The peak transconductance – g_{max} is found to slightly shift to a more positive V_{G} and decreases in magnitude [12,13].

The underlying metallurgical process causing the degradation of the electrical parameters in GaAs-based devices during accelerated life testing is generally attributed to the decrease in the SBL thickness caused by the Ti indiffusion. Other mechanisms have been suggested, such as a decrease in the layer thickness due to the interdiffusion of the epilayers at the hetero-interface, [14] and Ga vacancy formation leading to charge redistribution in the SBL [11].

It is noted that other, different materials-based PHEMT devices, have been shown to exhibit promising thermal stability [15]. However, long term thermal stability needs further investigation.

Despite many publications regarding the gate sinking mechanism, a physical explanation is still lacking. The aim of this study was to quantitatively correlate the observed degradation of the electrical parameters with the physical processes caused during gate sinking. This is done by measurements and modeling.

2. Experimental details

The devices used for accelerated life testing were AlGaAs/InGaAs 0.25 μm gate devices. Device gates were standard Ti (40 nm)/Pt (40 nm)/Au (400 nm). Two different gate designs were used: symmetric and offset. The device's heterostructure consists of a spacer layer between the SBL and the active channel, full device heterostructure details are described elsewhere [16]. Two different device structures were used, with a SBL thickness of either 30 nm or 23 nm. In total, 25 devices were tested.

Accelerated life testing was performed at three different ambient temperatures – 120 °C, 145 °C and 170 °C (measured at the base plate), corresponding to channel temperatures of 232 °C, 264 °C, 296 °C, respectively. Channel temperatures were modeled using the Thermal Analysis System (TAS) of Harvard Thermal Inc. The model took into account the FET horizontal and vertical layout and vertical stack including solder and carrier. GaAs thermal conductivity dependence on temperature was also included in the simulation. Thermal resistance between carrier and heater was not included since adjusted surfaces were applied in the test [17]. Accelerated life testing was also performed under different gate biases ranging from $V_{\mathrm{G}} = -0.35$ V to -0.7 V. Drain bias was maintained at $V_{\mathrm{D}} = 7 \pm 0.15$ V. Under these bias conditions, the drain current is in saturation.

During life testing, the I_{Dsat} was monitored as the degradation parameter. The failure criterion, denoted as the Time-To-Failure (TTF), was chosen as the time in which the device exhibits a 10% decrease in drain current.

All devices passed burn-in prior to life testing to eliminate defective devices and for device stabilization. Burn-in conditions were the following: ambient temperature 90 °C, drain voltage $V_{\mathrm{D}} = 7 \pm 0.15$ V, gate voltage $V_{\mathrm{G}} = -0.53 \pm 0.05$ V, burn-in time was 160 ± 20 h. In addition to I_{Dsat} monitoring during testing, the devices

were occasionally cooled to room temperature for electrical characterization.

3. Degradation modeling

The following simplified analytical degradation model applies the parabolic rate law of the TiAs phase formation into the basic analytical PHEMT charge control model using necessary modifications. An analytical expression for the diffusion of Ti into the AlGaAs layer is also developed, providing finer details of the diffusion process. The model correlates the Ti diffusion rate, and thus the rate of the decrease in the SBL thickness due to the growth of the TiAs phase, with the V_P and I_{Dsat} degradation rates.

The drain current expression at saturation for short channel devices (Eq. (2)) was developed by Delagebeaudeuf and Linh [18] using the gradual channel approximation

$$I_{Dsat} = \frac{Z\varepsilon_i v_S}{d}(V_G - V_P - R_S I_{Dsat} - \varepsilon_f L) \tag{2}$$

where Z is the gate width, v_S is the electron saturation velocity, ε_i is the permittivity, d is the SBL thickness, V_G is the gate bias, R_S is the source resistance, ε_f is the saturation electric field and L is the gate length.

The pinch-off voltage depends on both material and device design. For a δ-doping design, it can be shown that V_P is proportional to the undoped AlGaAs layer thickness as empirically substantiated [19]. Thus,

$$V_P = \phi_b - \frac{\Delta E_C}{q} - \frac{qN_d(d - d_{spacer})}{\varepsilon_i} \tag{3}$$

where ϕ_b is the barrier height, ΔE_C is the conduction band discontinuity, q is the electronic charge, N_d is the doping concentration of the δ-doped layer and d_{spacer} is the spacer layer thickness.

As discussed earlier, the SBL thickness decreases with the growth of the TiAs phase during life testing according to $d = d_0 - W_{TiAs}$, where d_0 is the original SBL thickness. Eq. (3) shows that the reduction in the SBL thickness leads to a positive V_P shift. Since the TiAs phase continues to grow during annealing, d decreases, V_P becomes more positive, subsequently degrading I_{Dsat} as shown in Eq. (2).

Rewriting Eq. (2), we arrive at the following relation, [20]:

$$I_{Dsat} = \frac{Z\varepsilon_i v_S}{d + R_S Z\varepsilon_i v_S}(V_G - V_P - \varepsilon_f L) \tag{4}$$

Although I_{Dsat} is linearly proportional to the SBL thickness (through V_P in Eq. (3)), it is also proportional to its reciprocal in the term preceding the brackets in Eq. (4) (sometimes referred to as the external transconductance, g'_m). However, the SBL thickness in the latter term is less significant since the denominator is also a function of the $R_S Z\varepsilon_i v_S$ product.

It is noted that the Schottky barrier height changes with the formation of the TiAs phase causing a further shift in V_P, as understood from Eq. (3). However, the contribution of the Schottky barrier height shift to V_P degradation is comparably small since both contacts, i.e., Ti and TiAs on GaAs, have relatively similar barrier heights, as discussed earlier.

The diffusion profile of Ti in the SBL can be obtained using the solution of Fick's second law, [21]

$$C(x,t) = \frac{M}{\sqrt{\pi Dt}}\exp\left(-\frac{x^2}{4Dt}\right) \tag{5}$$

where M is the total diffusing mass, D is the diffusion coefficient, x is the distance from interface and t is the diffusion time.

The Ti layer of thickness $2h$ is confined between the Pt diffusion barrier and the SBL. The diffusion coefficient of Ti in Pt is virtually zero [22]. Thus, the diffusion of Ti into this layer may be neglected. The diffusion coefficient of Ti in GaAs, D_{GaAs}, is evaluated using the data given by Lee et al. [13] which are consistent with later data [23].

Adapting Eq. (5) to the structure at hand (see inset of Fig. 2), we arrive at Eq. (6) (see Appendix I), which shows that the Ti concentration profile is governed by a series of error functions

$$C(x,t) = \frac{C_0}{2}\left\{\mathrm{erf}\left(\frac{x+h}{2\sqrt{D_{GaAs}t}}\right) + \mathrm{erf}\left(\frac{h-x}{2\sqrt{D_{Pt}t}}\right)\right\} \tag{6}$$

where $x = +h$ and $x = -h$ are the positions of the Ti interfaces with Pt and the SBL, respectively, as shown in Fig. 2.

Fig. 2 shows calculated Ti concentrations (normalized) in the SBL as a function of the distance from the AlGaAs–Ti interface for annealing times between 0 and 250 h at a temperature of 145 °C. Similar profiles are found at different annealing temperatures although the rate of Ti penetration into the SBL increases exponentially with temperature. The TiAs phase forms as the Ti diffuses into the SBL. Since the Ti diffusion is rate limiting step, the TiAs profiles are expected to follow the Ti profiles in Fig. 2.

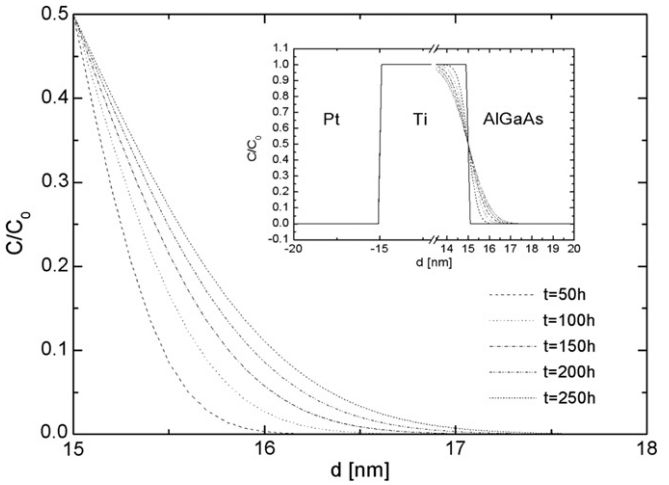

Fig. 2. Ti concentration in the AlGaAs layer as a function of distance from the Ti–AlGaAs interface. Each curve represents a different annealing time.

4. Results and discussion

Fig. 3 shows the I–V characteristics, measured at room temperature and at a gate voltage $V_G = -0.4$ V, of a sample life tested at an ambient temperature $T = 145$ °C. The other samples produced similar curves.

Fig. 4 shows I_{Dsat} (somewhat vertically shifted for a uniform starting point) as a function of time for the samples during life testing at three different annealing temperatures as well as gate and drain bias conditions. The curves at each temperature are bunched together. The modeled I_{Dsat} curves, according to Section 3, are also shown in Fig. 4 for each testing temperature (120 °C – open circles, 145 °C – open triangles, 170 °C – open diamonds). All devices exhibited continuously decreasing I_{Dsat} with time until failure. Using the 10% I_{Dsat} decrease failure criterion, TTF values of the devices were extracted. The TTF values were plotted as a function of temperature yielding an exponential curve. The Arrhenius relation was used to calculate the activation energy of the degradation mechanism from the curves (not shown). The activation energy was determined to be 1.6 ± 0.1 eV. This value corresponds to the activation energy of the gate sinking mechanism as discussed in Section 1.

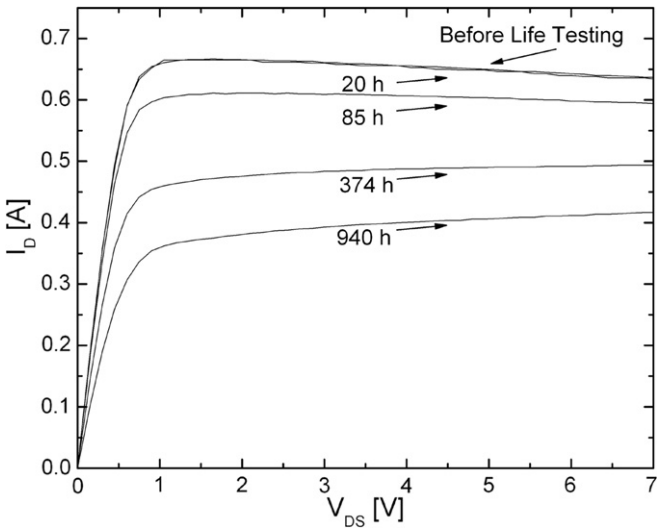

Fig. 3. I–V characteristics of a device measured at room temperature and at a gate voltage $V_G = -0.4$ V, life tested at an ambient temperature $T = 145$ °C.

Fig. 5 shows the drain current, I_D, at $V_D = 0.3$ V, as a function of V_G, extracted from I_D to V_D measurements, at different times during accelerated life testing of a device annealed at a temperature of 120 °C. The inset shows a zoom-in on the portion of V_G between -0.6 V and -1.1 V. The I_D–V_G curves were used to find V_P by extrapolation in the linear region method (ELR), [24] in which the intersection of the extrapolated linear part of the curve with $I_D = 0$ yielded V_P. The pinch-off voltage continuously shifted with time during annealing to a more positive value. The extraction of V_P was performed on several other devices of Fig. 4 at different life testing temperatures.

Examination of the extrapolated lines of Fig. 5 in finer detail shows that the slopes, corresponding to g'_m, change only slightly in comparison with the V_P shifts of the same lines. This behavior is observed also for other devices of Fig. 4 life tested at different annealing temperatures. This indicates that the main cause of the decrease in I_{Dsat} (see Eq. (4)) is due to the V_P term rather than the g'_m term.

Fig. 6 shows V_P as a function of time during life testing at 3 annealing temperatures as well as gate and drain bias conditions. The curves at each temperature are grouped

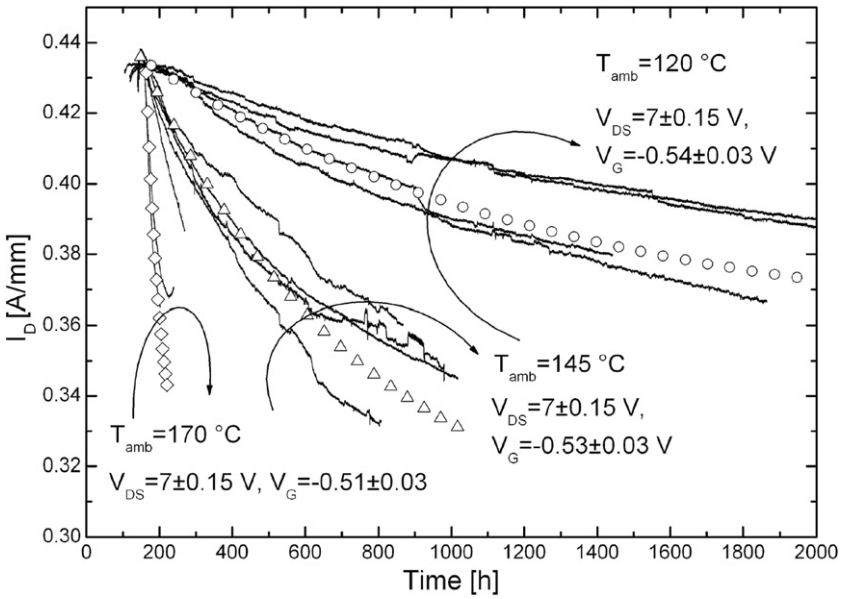

Fig. 4. Measured saturation drain currents (somewhat vertically shifted for a uniform starting point) of the various devices during accelerated life testing (solid curves) in comparison to the models at the different temperatures (120 °C – open circles, 145 °C – open triangles, 170 °C – open diamonds).

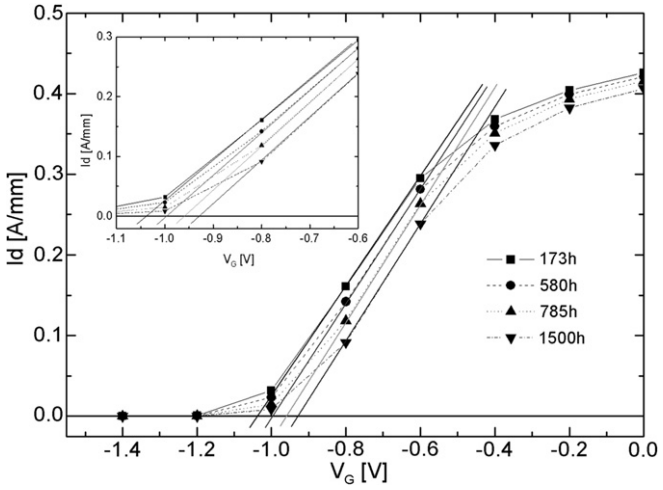

Fig. 5. Drain current vs. gate voltage curves used to determine V_P by the ELR method.

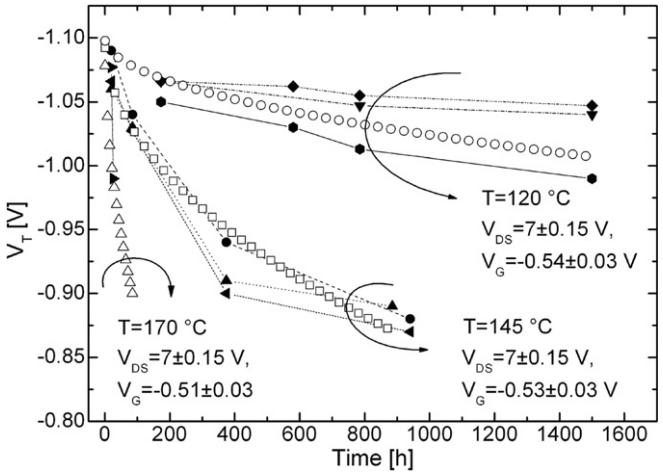

Fig. 6. The Pinch-off voltage as a function of time at different annealing temperatures. The curves with symbols (120 °C – open circles, 145 °C – open squares, 170 °C – open triangles) represent the modeled V_P degradation and the dashed curves – the calculated V_P.

together. The modeled V_P curves, according to Section 3, are also shown in the figure for each testing temperature (120° – open circles, 145 °C – open squares, 170 °C – open triangles). All the tested devices showed a continuous V_P shift to a more positive value during life testing. The rate of the V_P shift increases with temperature.

The activation energy for the V_P degradation mechanism was obtained similarly as for I_{Dsat}. The 'failure criterion' was chosen as the time (TTF) for a 10% shift of V_P from its initial value. The results were plotted as a function of temperature (not shown). Using the Arrhenius relation, the activation energy was determined to be 1.8 ± 0.3 eV, which suggests that V_P degrades, similarly as I_{Dsat}, by the gate sinking mechanism.

The measured I_{Dsat} failure time at each annealing temperature was used in the I_{Dsat} model. At the annealing temperatures of 145–170 °C, failure was met at an average SBL thickness decrease of about 2 nm, whereas at 120 °C, failure occurred at a SBL thickness decrease of about 1.5 nm. This discrepancy may be explained by a second degradation mechanism, such as Ga vacancy formation favored at lower temperatures, as suggested in Ref. [10]. As the testing temperatures increase, the TiAs phase formation becomes the dominant mechanism.

During accelerated life testing, I_{Dsat} of devices with smaller SBL thickness degraded faster compared to those having thicker SBLs. This result is similar to that reported in Ref. [3], where devices having a more negative initial V_P value, denoting a thicker SBL, degraded more slowly while the Ti sinking depth was similar for all devices, regardless of their initial V_P value. This behavior may be explained by applying the model suggested in Section 3. The pinch-off voltage and approximately I_{Dsat} are linearly proportional to the SBL thickness. The relative thickness change of degrading devices, having an initially thin SBL, is greater than that of thicker SBL devices. Hence, the I_{Dsat} degradation rate of a thinner SBL device appears to be enhanced compared to a similar device with a thicker SBL though the physical damage (the SBL decrease) is similar in both devices.

Thus, the relative decrease in I_{Dsat} (e.g., 10%) as a failure criterion provides only limited information regarding device reliability. Monitoring the V_P shift through frequent I_D–V_D characterization during life testing may serve as a better indicator for device robustness to gate sinking since it directly reflects the physical damage caused by gate sinking, i.e., the SBL thickness decrease. Additionally, unlike I_{Dsat}, V_P is not affected by parasitic resistances, which change during annealing.

5. Conclusions

A simple analytical model for PHEMT device degradation during accelerated life testing is presented. The gate sinking mechanism is caused by Ti diffusion into the SBL and the subsequent growth of the TiAs phase, which leads to the decrease in the SBL thickness. This results in shifting of V_P to more positive values and decreasing I_{Dsat}. Devices with smaller SBLs are less robust compared with those having thicker SBLs because the relative decrease in thickness of thinner SBL devices is greater. It is suggested that the V_P shift may be used as the failure indicator rather than the relative decrease in I_{Dsat}. The model makes it possible to calculate the decrease in the SBL thickness and I_{Dsat} degradation.

Appendix I. Solution of Ti diffusion into the AlGaAs layer

The solution for Fick's second law is given in Eq. (5). The boundary conditions at $t = 0$ are

$$-h < x < +h, \quad C_{Ti} = C_0;$$
$$x < -h,\ x < +h, \quad C_{Ti} = 0;$$

where $h = 0.25/2\ \mu m$ $x < -h$, diffusion coefficient D_{Pt}; $x < +h$, diffusion coefficient D_{GaAs}.

We sum the contributions of every thin sheet of Ti in the metal layer, of thickness $\delta\zeta$ and a distance ζ to a point p in the AlGaAs layer. Thus, the concentration at any time t at the point p is as expressed as follows:

$$C(p,t) = \frac{C_0 \delta\zeta}{2\sqrt{(\pi D t)}} \exp\left(-\frac{\zeta^2}{4Dt}\right) \tag{7}$$

where C_0 is the Ti concentration at the interface.

Integrating over the thin Ti sheets we write

$$\begin{aligned} C(x,t) &= \frac{C_0}{2\sqrt{(\pi D t)}} \int_{x-h}^{x+h} \exp\left(-\frac{\zeta^2}{4Dt}\right) \mathrm{d}\zeta \\ &= \frac{C_0}{\sqrt{\pi}} \int_{\frac{x-h}{2\sqrt{D_{Pt} t}}}^{\frac{x+h}{2\sqrt{D_{AlGas} t}}} \exp(-\eta^2)\mathrm{d}\eta \end{aligned} \tag{8}$$

where $\eta = \frac{\zeta}{\sqrt{4Dt}}$, changing the boundary conditions accordingly.

Finally, we use the error function definition $\mathrm{erf} z = \frac{2}{\sqrt{\pi}} \int_0^z \exp(-\eta^2)\mathrm{d}\eta$ the error function property, $\mathrm{erf}(-z) = -\mathrm{erf}(z)$ and that

$$\begin{aligned} &\frac{C_0}{\sqrt{\pi}} \int_{\frac{x-h}{2\sqrt{D_{Pt} t}}}^{\frac{x+h}{2\sqrt{D_{AlGas} t}}} \exp(-\eta^2)\mathrm{d}\eta \\ &= \frac{C_0}{\sqrt{\pi}} \left(\int_0^{\frac{x+h}{2\sqrt{D_{AlGas} t}}} \exp(-\eta^2)\mathrm{d}\eta - \int_0^{\frac{x-h}{2\sqrt{D_{Pt} t}}} \exp(-\eta^2)\mathrm{d}\eta \right) \end{aligned}$$

and arrive at Eq. (6).

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