Nonuniform RF Overstress in High-Power Transistors and Amplifiers

Alon Stopel, Mark Leibovitch, and Yoram Shapira, *Senior Member, IEEE*

***Abstract*—Nonuniform light emission from power transistors at 2–3-dB compression levels has been imaged using a microscope-mounted camera. The nonuniformity depends on the device lateral geometry, load impedance, dc and radio frequency (RF) conditions, and the negative gate current, which is a result of the RF-induced impact ionization in the transistors. Numerical simulations demonstrated a nonuniform distribution of the RF overstress in the transistors under the same conditions. The simulations indicate that the nonuniformity in the light intensity may be attributed to the RF-induced voltage overstress. Therefore, the observed light emission may be used as a direct and contactless monitor of the RF-induced overstress in transistors and power amplifiers.**

***Index Terms*—Breakdown, high-power amplifier (HPA), impact ionization (II), light emission, parasitic oscillations, power transistor.**

I. Introduction

THE PERFORMANCE of high-power amplifiers (HPAs) is continually being improved in terms of power density, efficiency, and gain, without any reduction in the reliability requirements [1], [2]. The efforts in this direction have become a major driving force of device evolution with a focus on device structure and material composition. Usually, power transistors are comprised of a number of transistor unit cells (fingers) that are connected in parallel. The number and width of the fingers are mostly dictated by the application and frequency range, whereas the internal device structure is strongly dependent on the device technology. The individual device fingers are connected in parallel by interdigital electrodes, such that a large number of loops are formed between the transistor fingers. The loops may lead to a nonuniform distribution of the resultant voltage $(V_{\rm RF})$ across a loop, which is strongly affected by internal reflections in the device and mismatch effects. In some cases, nonuniformity in $V_{\rm RF}$ occurs due to parasitic oscillations excited under actual operational conditions [3].

Recently, we presented a possible correlation between nonuniform radio frequency (RF) overstress and nonuniform light emission in high-power transistors at the 2–3-dB compression level [4]. The light emission is caused by impact ionization (II) processes. One of the factors that influence the II level is the RF stress. Monitoring the spatial distribution of $V_{\rm RF}$ in the power transistor under actual operational conditions is of great importance because it may yield a deep insight into the overstress distribution in a device. In this paper, we propose an empirical model based on the experimental data. We find it in agreement with a numerical simulation model describing the behavior of the same devices under dc and RF operational conditions. We show the use of a photon-emission-based methodology for monitoring the distribution of electrical stress in a power transistor and in HPAs [5]–[7]. This stress is a strong function of the device structure and the operational conditions, particularly the output impedance $(Z_{\rm out})$. The emitted light distribution appearing in the device under test (DUT) reflects II processes across the device.

The technique may be applied to any solid-state HPA technology, without losing the universality of the approach. In this paper, the technique is demonstrated and evaluated for the mature pseudomorphic HEMT (PHEMT) device technology presented by an HPA at 10 GHz.

Section II describes the device structure, the experimental setup, and the software tools. The measurement results and empirical modeling are discussed in Section III. Section IV presents the numerical simulation process and the matching between the simulation-based model and the empirical measurements. The conclusions are presented in Section V.

II. Experimental

For a power transistor, the impact of the device geometry on the performance is a challenging task because of significantly nonlinear phenomena in the underlying device physics [8], [9]. The power transistors are comprised of a number of transistor unit cells (fingers) connected in parallel by interdigital electrodes. An optimum cell-paralleling scheme, which is required for high power, must account for a complex interplay between the principles for the best thermal and microwave designs. The selection of the transistor size, gate width, and number of fingers strongly depends on the frequency range and the application. A proper layout for reducing the operating temperature must consider individual finger width and separation between fingers—gate-to-gate pitch (D_p), substrate thickness.

The power transistor microwave performance is usually assumed to depend on the unit cell lateral geometry. In the HEMT device, it includes gate recess $(L_{\rm wr})$, drain-source spacing $(L_{\rm ds})$, gate-recess spacing $(L_{\rm wr,g})$, source- recess spacing $(L_{\rm s,wr})$, and gate length $(L_{\rm g})$. The key lateral layout parameters of a transistor are shown in Fig. 1. These lateral parameters set

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The authors are with the Department of Physical Electronics, School of Electrical Engineering, Tel-Aviv University, Tel Aviv 69978, Israel (e-mail: stopel-a@013.net).

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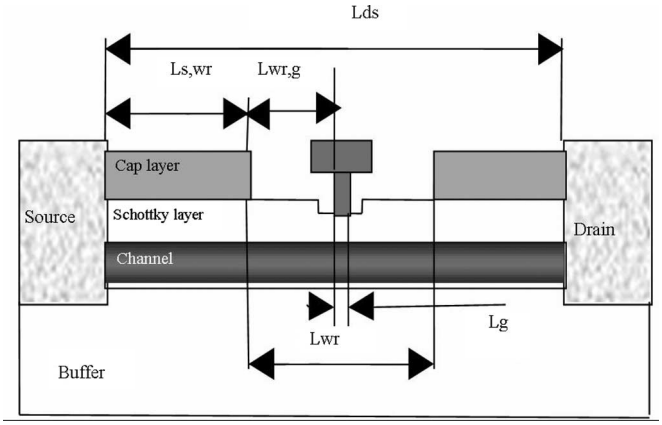

Fig. 1. Double-recessed HEMT.

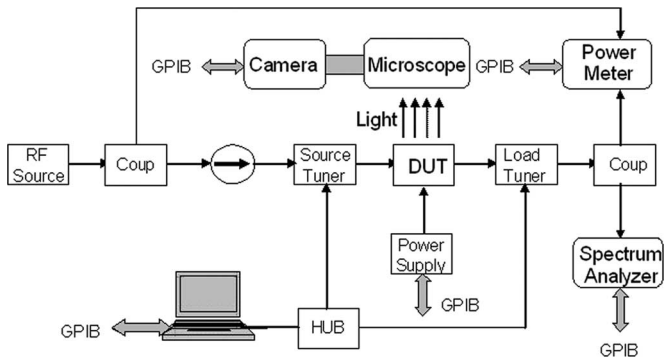

Fig. 2. Load-pull and light emission measurement setup.

the interplay between the electric fields in the transistor at the desired working point under dc and RF conditions.

The statistical design of experiment (DOE) approach to transistor design allows the derivation of correlations between device performance and geometry [8], [9]. The DOE method makes it possible to design a device matrix with different lateral and structural geometrical parameters. Thus, correlations between the geometrical parameters and measured electrical characteristics can be statistically established.

The variables for the device matrix were based on a combination of the key lateral layout parameters of the power HEMT. The two-level device matrix makes it possible to model the electrical characteristics of the matrix, taking into account the entire first- and second-order effects. Without loss of generality [10], [11], the following ranges of five key layout parameters have been chosen, in our case, to optimize a 10-GHz HPA: $L_{\rm g} = 0.2{-}0.3\ \mu$m, $L_{\rm wr} = 1.4{-}1.7\ \mu$m, $L_{\rm ds} = 3{-}3.5\ \mu$m, $L_{\rm wr,g} = 0.4{-}0.6\ \mu$m, and $L_{\rm s,wr} = 0.7{-}0.9\ \mu$m.

To evaluate the transistor power performance, the output power and power-added efficiency (PAE) figures of merit have been used. These figures make it possible to compare the transistor performances and select the best device for a given specific application.

The limiting mechanism of the power performance is the transistor breakdown (characterized by the breakdown source-drain voltage $V_{\rm br}$) that is marked by a sharp increase in the gate/drain current [12], [13]. $V_{\rm br}$ is defined through a direct measurement where the negative gate current (I_g) reaches a magnitude of 1 mA/mm (assuming that I_g is uniformly distributed across the transistor unit cell). The increase in I_g is due to minority carriers (holes), which are generated by the II process [12], [13]. This process entails free carrier generation in a region of the transistor, where the resultant electric field is above a critical value $(F_{\rm critical})$. Recombination of the free carriers may lead to light emission from the device during II [14], [15], which has been observed for various device technologies [14], [16]–[18].

In the large device, the fingers are connected in parallel in an interdigital structure where the distance between the transistor fingers and output terminals becomes a function of the finger position. There are operational conditions under which nonuniformity in $V_{\rm RF}$ and parasitic oscillations in the transistor fingers may appear. A number of techniques have been developed to eliminate the nonuniform distribution of the resultant voltage $(V_{\rm RF})$ and the parasitic oscillations at the chip and at the device level [19], [20]. This paper is focused on monitoring the spatial RF voltage distribution in the power transistors and on determining the origin of the nonuniformity of the stress buildup in the devices. This is done under actual operational conditions by using light emission as a fingerprint of voltage overstress. This device matrix makes it possible to demonstrate the proposed approach for 10-GHz-HPA monitoring, as well as the underlying physics through the extraction of empirical models for the key power parameters.

The setup consists of a number of basic blocks: dc power supply, RF Source, passive load pull, optical system, and a computer. Fig. 2 shows a schematic representation of the setup.

All DUTs passed through screening procedures that uses dc and RF measurements. In addition, the electrically active defects were monitored by photoemission inspection under dc conditions. The following power measurements were performed on "defect-free" devices, with dc and small-signal parameters that comply with device specifications. Using electromechanical tuners, on-wafer load-pull measurements have been used to obtain the $P_{\rm in} - P_{\rm out}$ characteristics of a DUT at 10 GHz in a variety of dc operation ranges ($V_{\rm ds} = 5{-}9$ V, $V_{\rm gs} = -1.1$ to -0.6 V, and the typical $V_{\rm br}$ being higher than 18 V) for a number of input/output impedances. The region of output impedances ($R = 10{-}35\ \Omega$ and $jX = -12$ to $18\ \Omega$) covers the vicinity of the optimal impedances. The load tuners were selected to provide the best matching for maximum power, corresponding to ∼2–3-dB gain compression under actual operation conditions.

For each transistor under test, output power, efficiency, gain, gate/drain currents, as well as photon emission data, were collected. All electrical measurements were performed on the wafer using an HP 4155 C semiconductor analyzer and an 8510 C network analyzer and a passive load pull. A Sony XC555 P camera and an Optem Zoom70 XL microscope were used for taking the photon images under RF load and dc conditions. A Hypervision photon-emission microscope (Visionary 2000) was used for photon collection under dc conditions.

Photoemission images were processed using MATLAB. The statistical analysis of the data was carried out using a Statistical Analysis System software (JMP 5.0). Numerical simulation

and analysis were carried out by using Advanced Design System (ADS) and JMP.

III. Measurement Results and Empirical Modeling

DC and RF data have been collected during typical load-pull measurements of the set of devices. In addition, light emission mapping was performed. It has been found that the light emission intensity increases and becomes significant when the RF signal is increased. In the vicinity of power compression points, the increase in the negative gate current is accompanied by the appearance of a significant light emission, which is clearly nonuniform under certain operational conditions. Fig. 3(a) shows the light intensity as a function of finger position for a 2–3-dB compression. The inset presents an image of the emitted light superimposed on the transistor layout. The dashed line marks the cross section. Fig. 3(b) and (c) shows an example of a light emission distribution across an entire power transistor comprised of two additional transistor unit cells with different layout parameters and under various electrical conditions. The light intensity nonuniformity may be described using $\Delta I_{\rm light} = I_{\rm MAX} - I_{\rm MIN}$ (where $I_{\rm MAX}$ represents the maximum light intensity and $I_{\rm MIN}$ the minimum light intensity across the entire transistor).

For the entire set of devices under the tested operational conditions, the output power is changed in the range of 27.5–30.5 dBm. The PAE changed in the range of 35%–65%, the negative gate current was in the range of 0–3 mA, and light nonuniformity was in the range of 0–140 (in arbitrary units) [4]. The relations between the measured parameters may be represented through the correlation coefficients shown in Table I.

The output power $(P_{\rm out})$ may be approximated by the following empirical linear expression $(R_{\rm square} = 91\%)$:

$$P_{\rm out}\ [\rm dB] = 26.3 - 0.08 \cdot \Delta I_{\rm light} + 0.41 \cdot V_{\rm ds}. \qquad (1)$$

The impact of the drain voltage on $P_{\rm out}$ is expected and leads to an increase of the output power by 0.4 dB per each additional volt. On the other hand, the reduction of $P_{\rm out}$ is accompanied by an increase in light nonuniformity, which clearly indicates that $\Delta I_{\rm light}$ is due to the parasitic effects in the transistor. Fig. 4 shows light intensity as a function of the output power and PAE. Fig. 3 shows that $P_{\rm out}$ and PAE decrease when $\Delta I_{\rm light}$ increases. A possible origin will be discussed in Section IV.

To understand the physics behind the parasitic phenomena, we have performed empirical modeling of I_g and $\Delta I_{\rm light}$. There is a consensus that the negative gate current (I_g) indicates II processes in the power transistor [12], [14], and it is expected to be a strong function of geometrical parameters, as well as operational conditions [21]. In the experiment of interest, RF power swings drive the transistor out of the safe operational region [13], which is defined as the region where the gate current is higher than -1 mA/mm. Out of the safe operational region, the II degrades the device performance and leads to the significant generation of excess carriers, which contribute to the negative gate current. Depending on the device geometry, load

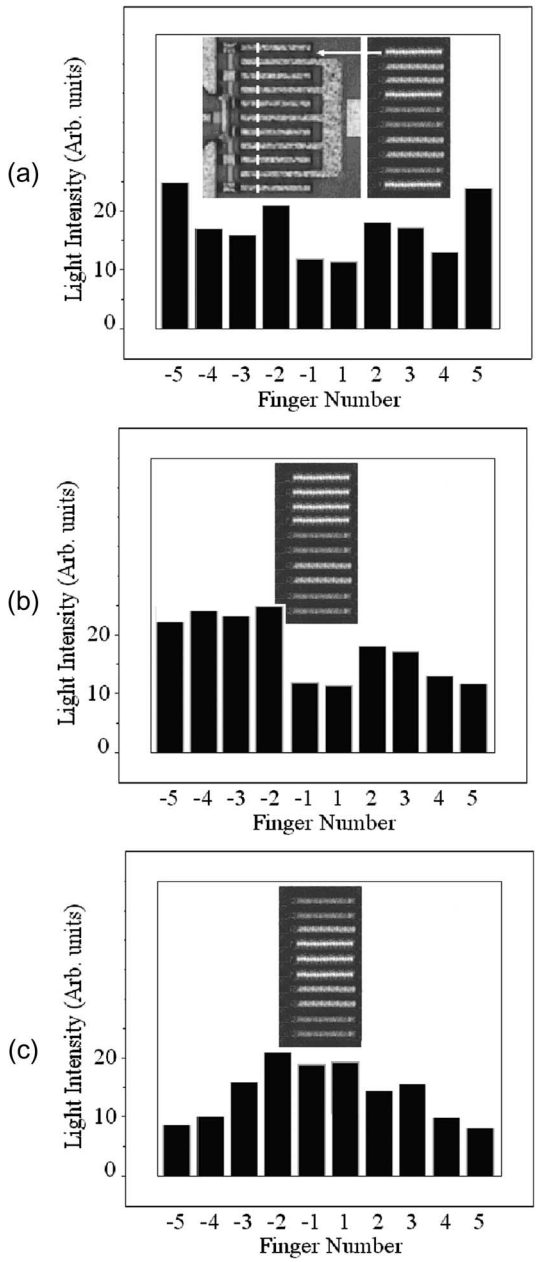

Fig. 3. Example of a light emission distribution across an entire transistor for three cases of different layout parameters and various electrical conditions. Inset: Image of the emitted light superimposed on the transistor layout. The dashed line in (a) marks the cross section.

impedance, and operational voltage, a device may be driven into one of the states where a combination of the electrical fields and electrical currents trigger the generation process. Thus, it is expected that I_g depends on $Z_{\rm out}(R, jX)$, $V_{\rm ds}$, and the layout parameters. Using the given set of devices, the I_g empirical model can be expressed by $(R_{\rm square} = 93\%)$

$$\begin{aligned} I_g = {} & 111 \cdot L_{\rm g} - 103 \cdot L_{\rm s,wr} - 11685 \cdot (L_{\rm g} - 0.23) \\ & \cdot (L_{\rm s,wr} - 0.735) + 27 \cdot L_{\rm wr} - 3146 \cdot (L_{\rm g} - 0.23) \\ & \cdot (L_{\rm wr} - 1.43) - 3.8 \cdot R + X \cdot 3.8 - 22.5 \cdot V_{\rm ds}. \end{aligned} \qquad (2)$$

In the range of drain voltages of 6–9 V, an increase in $V_{\rm ds}$ leads to a rise in the magnitude of the negative gate current

TABLE I
CORRELATION COEFFICIENT MATRIX FOR $V_{\rm ds}$, PAE, $\Delta I_{\rm light}$, AND $P_{\rm out}$

	V_{ds} [V]	PAE [%]	ΔI_{light} [Arb Units]	P_{out} [dB]
V_{ds} [V]	1	-0.371	0.316	0.677
PAE [%]	-0.371	1	-0.824	0.207
ΔI_{light} [Arb Unit]	0.316	-0.824	1	-0.174
P_{out} [dB]	0.677	0.207	-0.174	1

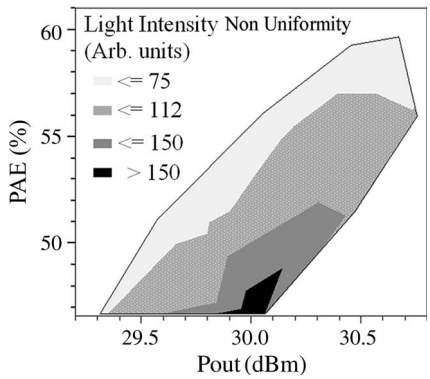

Fig. 4. Light intensity as a function of output power and PAE.

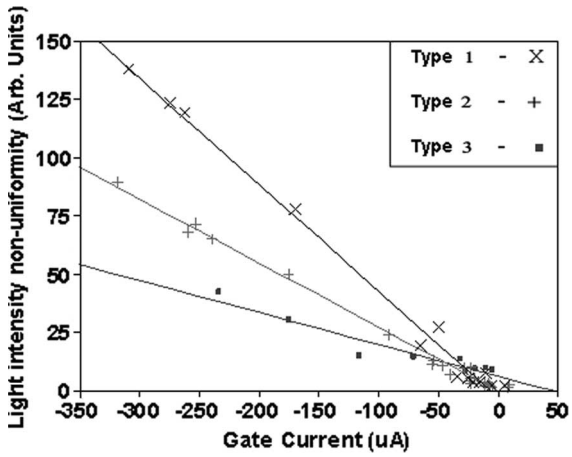

Fig. 5. Light intensity nonuniformity ($\Delta I_{\rm light}$) as a function of I_g for a 2–3-dB compression for three groups of devices with significantly different layout parameters.

due to a higher initial electric field in the DUT. The impact of $Z_{\rm out}(R, jX)$ is represented by the effects of the real and imaginary parts on I_g. It is observed that the magnitude of I_g is increased with increased R, which is the load resistor, and for negative values of X.

The layout parameters $L_{\rm g}$, $L_{\rm s,wr}$, and $L_{\rm wr}$ have pronounced impact on the distribution of the electric field in the device. In the case under consideration, the most significant contribution comes from the interaction between $L_{\rm g}$ and $L_{\rm s,wr}$. The interaction between $L_{\rm g}$ and $L_{\rm wr}\cdot L_{\rm g}$ and $L_{\rm s,wr}$ define the electric field in the source-gate region, which may trigger the II in this region. On the other hand, the gate-recess width and depth are affected by the interaction between $L_{\rm g}$ and $L_{\rm s,wr}$. This effect is typical for the double-recess technology where the resulting gate length is defined through an aggressive lithographical process on the complicated topology of a device in the vicinity of the channel recess (represented by $L_{\rm s,wr}$). The thickness of the photoresist and gate length opening become a function of the topology for the given exposure time. The $L_{\rm g}$ and $L_{\rm wr}$ parameters define the resultant electrical field in a device, particularly in the gate-drain region. It is expected that an increase in these parameters will lead to the reduction of the electric field strength, resulting in the reduction, if any at all, of the negative gate current.

An insight of the physical phenomena behind nonuniform light emission may be achieved through numerical and empirical modeling. The starting point of this consideration is the correlation between the negative gate current and nonuniformity in the light emission intensity ($\Delta I_{\rm light}$). Fig. 5 shows this correlation for the three groups of devices with significantly different layout parameters. The following empirical expression for $\Delta I_{\rm light}$ fits the measured data ($R_{\rm square} = 90\%$):

$$\Delta I_{\rm light} = -0.065 \cdot I_g - 6.5 \cdot (L_{\rm s,wr} + L_{\rm wr,g}) + 12 \cdot L_{\rm wr}. \quad (3)$$

The strong nonuniformity in light distribution is observed in devices with a pronounced negative gate current only, which usually accompanies II processes in the device. The effect of the layout parameters $L_{\rm s,wr} + L_{\rm wr,g}$ and $L_{\rm wr}$ may be understood from the following consideration. For the set of devices under consideration, $L_{\rm s,wr} + L_{\rm wr,g}$ shows no pronounced impact on I_g (2) and, consequently, does not significantly affect the II processes. On the other hand, $L_{\rm s,wr} + L_{\rm wr,g}$ strongly affects the input and output reflectance coefficients [10], i.e., the matching of properties of the device. The empirical model shows that an increase in $L_{\rm wr}$ leads to the increase in $\Delta I_{\rm light}$. It is quite a surprising behavior. It is expected that an increase in $L_{\rm wr}$ would lead to the reduction of the carrier generation rate by II and, as a result, to the reduction in both the magnitudes of I_g and $\Delta I_{\rm light}$. The "strange" increase in light nonuniformity with $L_{\rm wr}$ indicates a different mechanism, which may originate in the impact of the $L_{\rm wr}$ on the output impedance of the transistor [21]. Thus, the layout parameters in (3) may affect the input/output impedances of the device and, consequently, the reflected RF power into the device from the external impedance $Z_{\rm out}(R, jX)$. A similar behavior has been observed by Khramtsov *et al.* [10] for the small signal S-parameters, where

an increase in $L_{\rm wr}$ and a decrease in $L_{\rm s,wr} + L_{\rm wr,g}$ led to the mismatch degradation of S_{22}.

Thus, for a large transistor, the derived empirical model for $\Delta I_{\rm light}$ indicates a direct correlation between light nonuniformity and the layout parameters facilitating the transistor output/input impedances. In Section IV, a detailed physical picture is constructed. It is based on an extensive numerical analysis where simulation results are used to estimate the feasibility of the proposed scenario under actual operational conditions.

IV. Numerical Simulation of the Load-Pull Measurements

The numerical simulation of the load-pull measurements makes it possible to get an insight about the underlying physical processes in a device. As mentioned above, in the large device, fingers are connected in parallel in an interdigital structure where, in the X-band, the "bar" type interconnection is used as the drain manifold and gate feed. The distance between the finger and output/input terminals becomes a function of the finger position, and the output/input impedances seen by each finger is inherently different. Therefore, the mismatch is expected to be a function of the finger position. The resultant spatial distribution of RF voltage is shaped through multiple reflections within a transistor (from the output/input terminals, as well as from other device fingers). $V_{\rm RF}$ may become significantly nonuniform across the entire transistor. Under actual operational conditions, the resultant $V_{\rm RF}$ at some fingers may exceed the breakdown threshold and lead to the generation of the excess electron-hole (e-h) pairs through II at these regions. The following radiative recombination of e-h pairs manifests itself in a nonuniform illumination across the entire transistor. The device manifold may play a critical role in the mitigation of the differences in RF distribution between the fingers.

Extended numerical simulations of load-pull measurements have been performed for a number of transistors. The numerical experiment is performed under a variety of operational conditions $[Z_{\rm out}(R = 10\text{–}35\ \Omega, jX = -12\ \text{to}\ 18\ \Omega), V_{\rm ds}(6\text{–}9\ \text{V}), V_{\rm gs}(-1.1\ \text{to}\ -0.6\ \text{V})]$. The simulation has been carried out for a typical device, i.e., a 10-finger device with an "interdigital bar"-type gate and a drain manifold. Each finger is represented using the nonlinear EEHEMT1 model (out of the ADS software library), which is based on the electrical parameters of our device matrix [22]. The cells are interconnected by a network of transmission lines, which fully reflect the topology and dimensions of an actual manifold—a gate-to-gate pitch D_p ($D_p = 26{-}40\ \mu$m) and an interconnect width of $W = 10{-}30\ \mu$m.

The simulation parameters have been arranged based on a two-level fractional DOE, which made it possible to define the major effects, as well as the interactions. During the load-pull simulation, the drain and gate voltages $(V_{{\rm D}i}, V_{{\rm G}i})$ and currents $(I_{{\rm D}i}, I_{{\rm G}i})$ of each finger, as functions of time, have been calculated (i states the finger number in the transistor). This was done in addition to the calculation of the total output power, voltage $(V_{\rm tot})$, and current. Under large signal conditions, the current–voltage dependence for the entire transistor has a typical elliptical shape [22]. Fig. 6 presents this shape of the I–V curve.

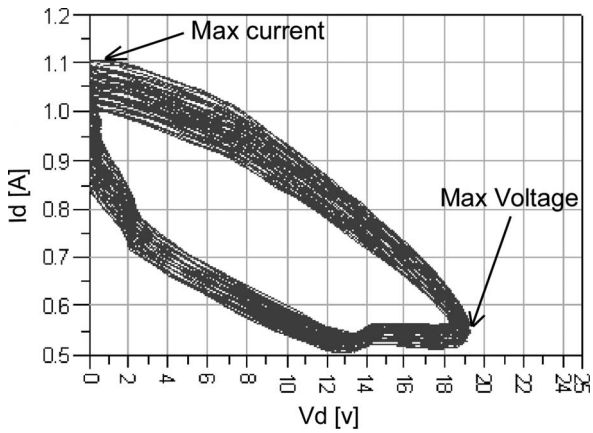

Fig. 6. Typical elliptical shape of the I–V curve.

The numerical simulation yields a unique possibility to get an insight into the distribution of the voltage across the entire transistor. It is found that the magnitude of the drain voltage $V_{{\rm D}i}$ may be a strong function of the finger position, and it may exceed the voltage detected at the transistor terminal $(V_{\rm tot})$. Fig. 7 shows the time dependence of $V_{\rm tot}$ and $V_{{\rm D}i}$ of two fingers, with extreme values of maximum voltage, for three different device structures and output impedances. Here, $V_{\rm Dhigh}$ is $V_{{\rm D}i}$ of the finger with the maximum drain voltage value, and $V_{\rm Dlow}$ is $V_{{\rm D}i}$ of the finger with the lowest maximum drain voltage. The simulation confirms that, under compression, the distribution of $V_{\rm RF}$ among the device fingers is highly nonuniform and may reach several volts, as shown in Fig. 7(a) ($Z_{\rm out} = 35 + j18\ \Omega$, $W = 25\ \mu$m, $L = 40\ \mu$m) and (b) ($Z_{\rm out} = 10 + j18\ \Omega$, $W = 20\ \mu$m, $L = 80\ \mu$m). Under different conditions, the distribution of maximum $V_{\rm RF}$ among the device fingers is almost uniform, as shown in Fig. 7(c) ($Z_{\rm out} = 20 - j12\ \Omega$, $W = 15\ \mu$m, $L = 120\ \mu$m). In addition to the simulated RF component of the gate current $-I_{{\rm G}i}$, the II current is estimated [23]–[25]. We have found that while the total negative current reaches -1.5 mA (from all the fingers), the negative gate current at a given finger, according to our simulation, could be in the range of -0.03 up to -0.92 mA (instead of the expected 0.15 mA in uniform case).

In the region (fingers) of high $V_{\rm RF}$, it may lead to severe II and a pronounced light emission, whereas the average emitted intensity across the device is low. Thus, light emission reflects the nonuniformity in $V_{\rm RF}$.

A model for the magnitude of the maximal difference between $V_{{\rm D}i}$ values has been derived from the numerical simulation. The value of $V_{{\rm D}i}$, integrated over one cycle, can be represented by $(R_{\rm square} = 96\%)$

$$\Delta V_{{\rm D}i} = |1.9 + 0.035 \cdot R + 0.05 \cdot X - 0.0035 \cdot (R - 14) \cdot (X - 23) + 0.12 \cdot W - 0.04 \cdot L| \quad (4)$$

where R and X are measured in ohms, whereas W is the width of the "bar" interconnect at the drain, and L is the distance between the device figures in step of D_p (both measured in micrometers). $\Delta V_{{\rm D}i}$ increases at low impedances (R, X) where manifold impact (longer and thinner transition lines) becomes pronounced. The model shows that for a typical 10-finger power

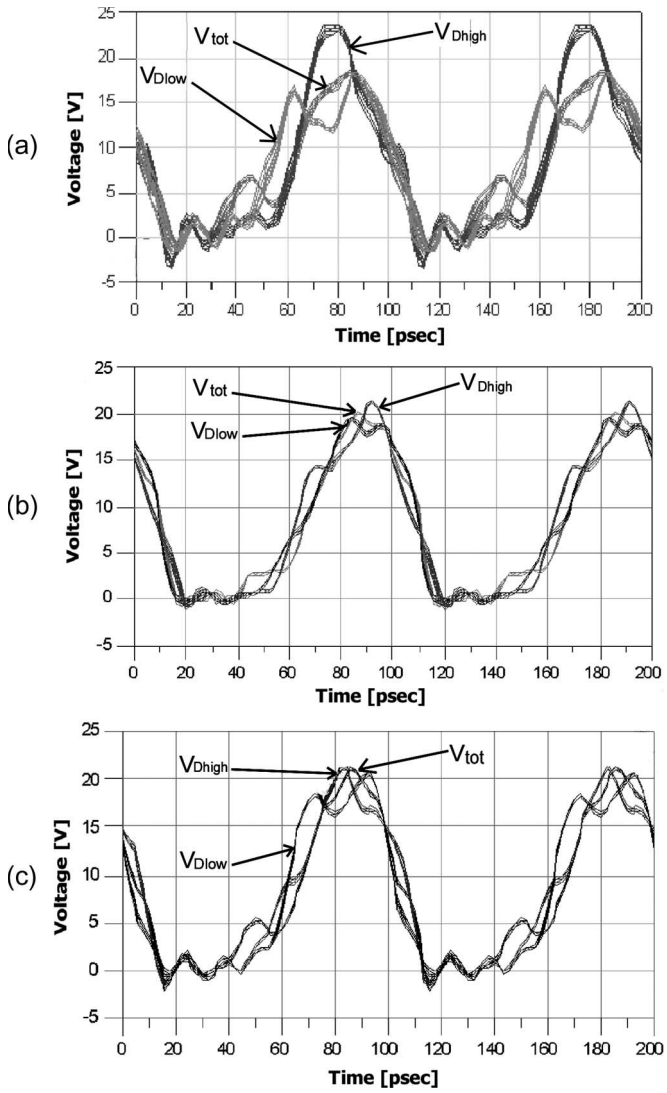

Fig. 7. Simulation results of $V_{\rm tot}$ and the two extreme values of $V_{{\rm D}i}$ occurring in two fingers over one cycle for the same device under three different operational conditions.

transistor, the distance between the central and outer fingers may lead to a $\Delta V_{{\rm D}i}$ of 2–5 V. On the other hand, an increase in the width of the manifold lines by 10 μm leads to a reduction in $\Delta V_{{\rm D}i}$ by 1.2 V.

As expected, the light nonuniformity distribution across the transistor measured at the experimental stage behaves according to the model derived from the numerical simulations in (4). In Fig. 3(a), the output impedance is $R = 30\ \Omega$ and $X = 18\ \Omega$, and the simulated $\Delta V_{{\rm D}i}$ is about 2.4 V. In Fig. 3(b), the output impedance is $R = 35\ \Omega$ and $X = 10\ \Omega$, and the simulated $\Delta V_{{\rm D}i}$ is about 3.9 V. In Fig. 3(c), the output impedance is $R = 10\ \Omega$ and $X = -12\ \Omega$, and the simulated $\Delta V_{{\rm D}i}$ is about 1.9 V. As expected, the nonuniformity distribution across the transistor fits the numerical simulation.

V. Conclusion

The results have shown that nonuniformity in light emission from power transistors strongly correlates with I_g at the 2–3-dB compression level and is a function of the device lateral structure and operational conditions. Numerical simulations have confirmed the nonuniformity of $V_{\rm RF}$ across the transistor fingers and the correlation of this nonuniformity with the transistor lateral structure and $Z_{\rm out}$.

The nonuniform emitted light may reflect the $V_{\rm RF}$-induced overstress and the II distribution across a transistor. Imaging the emitted light may be effectively used as a contactless $V_{\rm RF}$ overstress monitor at the transistor and chip levels.

The technique described in this paper can be used as a design quality testing and reliability assurance tool in the development phase of an HPA and as a part of RF testing of the HPA during the production phase. This technique easily highlights problems in the design and the production processes and may save considerable resources.

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Alon Stopel received the B.Sc. degree (*cum laude*) in electrical engineering from Technion, Israel Institute of Technology, Haifa, Israel, in 1989 and the MBA degree from Tel Aviv University, Tel Aviv, Israel, in 1994. He is currently working toward the Ph.D. degree at Tel Aviv University.

His current research interests include the optimization of power HEMT performance, contactless characterization, and modeling of HEMT for high-power high-frequency applications.

Mark Leibovitch received the M.Sc. degree in theoretical physics from the University of Tartu, Tartu, Estonia, in 1981 and the Ph.D. degree from Tel Aviv University, Tel Aviv, Israel, in 1995.

He is currently with the Department of Physical Electronics, School of Electrical Engineering, Tel-Aviv University. His current research interests include a wide variety of novel semiconductor devices and technologies, as well as contactless characterization techniques.

Yoram Shapira (M'98–SM'00) received the B.Sc. (with distinction) and D.Sc. degrees from Technion, Israel Institute of Technology, Haifa, Israel, in 1968 and 1973, respectively, both in physics.

After three years as a Research Associate with the University of Wisconsin, Madison, he has been with the Department of Physical Electronics, School of Electrical Engineering, Tel-Aviv University, where he is currently a Full Professor, incumbent of the Henry and Dinah Krongold Chair of Microelectronics. He has held numerous University and Faculty Committee positions, including Director of the Electrical Engineering Undergraduate Program from 1999 to 2002, Chairman of the University Admission Committee from 1991 to 1994, Electrical Engineering Department Head from 1987 to 1991, and member of the Steering Committee of the University Research Institute for Nanoscience and Nanotechnology, TAU from 1999 to 2003, etc. He was the founder and first Director of the Wolfson Applied Materials Research Centre from 1994 to 1997 and again from 2000 to 2005 and the Director of the Gordon Center for Energy Research from 1996 to 1997 and again from 2000 to 2005. He was the founder and first President of the Israeli Union of Materials from 1994 to 1997.

Prof. Shapira is a Fellow of the American Vacuum Society and an Honorary Member of the Israel Vacuum Society, having served as its Secretary (1982–1989) and President (1990–1992) and as the Israeli Representative and Councilor at the International Union for Vacuum Science for several terms.