Impact Ionization Measurements and Modeling for Power PHEMT

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***Abstract*—A systematic study of impact ionization in pseudomorphic high electron mobility transistors (PHEMTs) has been carried out using temperature-dependent electrical measurements as well as modeling for optimizing the power performance of the devices through the best layout parameters. A measurement procedure makes it possible to define a safe transistor operation region is proposed. Impact ionization in the channel is parameterized by specific gate current and voltage values. Temperature-dependent measurements are shown to provide distinction between the impact ionization current and the thermionic field emission current. A methodology for defining an optimum vertical structure and a lateral layout for a given application and operational conditions is developed. Empirical models for optimum lateral layout for a power application were developed based on a statistical "Device Zoo" approach. The results point to an optimal gate-to-drain distance for minimum impact ionization current.**

***Index Terms*—Breakdown, empirical models, impact ionization, pseudomorphic high electron mobility transistors (PHEMT).**

I. Introduction

PRECISE measurements and modeling of the on-state and off-state breakdown voltages in the pseudomorphic high electron mobility transistor (PHEMT) are needed due to its importance in power applications. Information about electrical breakdown is crucial for improvement of its power device performance since the breakdown limits the maximum transistor output power [1]–[3]. A number of works, published during the last decade [4]–[7], proposed various measurement methods and analytical models for the breakdown phenomenon. However, the design of a PHEMT with a predictable breakdown voltage remains a challenge.

The breakdown in PHEMTs is a complex phenomenon, dependent both on the geometry of the transistor and on the material properties of the initial wafer epitaxial layers. The breakdown manifests itself in a rapid increase of the gate current [8]. From the physical point of view, this current rise reflects either carrier generation processes occurring within the channel, or carrier transport, across the Schottky barrier, as well as both effects simultaneously. Carrier generation may be due to, e.g., impact ionization, which is the main generation process responsible for the breakdown [7], [9], Poole–Frenkel effect, or thermal generation [10] whereas transport across the Schottky barrier is carried out by thermionic field emission (TFE) or tunneling.

Both impact ionization and transport across the barrier relate to the electric field distribution in the PHEMT active region-channel and Schottky layer. Since impact ionization is inversely proportional to the bandgap [10], the channel is the weakest point of the PHEMT. This is because the channel bandgap has to be lower than the Schottky layer bandgap to provide good electron confinement within the channel [11]. In addition, good transport properties are associated with narrow bandgap material. Therefore, the maximal magnitude of the electric field in the channel controls the impact ionization process, while the TFE is controlled mostly by the electric field in the Schottky layer. The electric field magnitude and distribution in the channel, under constant bias voltages, can be varied by altering the lateral and vertical geometry of PHEMT.

This paper aims at optimizing power PHEMT performance. This is done by defining a safe PHEMT measurement methodology, which unambiguously separates between the TFE and impact ionization processes; parameterizing the impact ionization process for modeling; and developing an empirical model of the breakdown. The latter takes into account the effects of the vertical and lateral device geometry, as well as the doping level, on the breakdown at a given channel bandgap.

Since several geometrical parameters and their interaction impact the breakdown, a statistical approach has been used to derive an empirical breakdown model. Details of the experimental setup and statistical method, used in the research, are reported in Section II. The methodology, adopted for this study, is presented in Section. III. In this section, we prove that the two main physical processes, responsible for breakdown, can be separated. We also explain how the impact ionization can be parameterized. The results, discussion and empirical models of breakdown are presented in Section IV.

II. Experimental

A 0.25 μm gate power PHEMT was used as the basic element for this research. Fig. 1 shows a typical cross section of such a PHEMT indicating the key geometrical layout parameters. They are: L_{ds}-source-drain distance, L_{sg}-source-gate distance, L_{sr}-source-recess distance, L_r-recess width, and L_g-gate length. The main process steps include: A double heterostructure GaAs/AlGaAs/InGaAs MBE-grown initial wafers, which incorporate double Si planar delta doping, conventional alloyed AuGeNiAu Ohmic contacts, and a double-recessed submicron T-gate.

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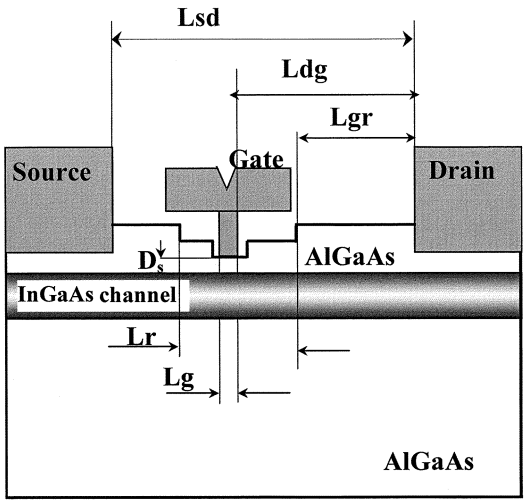


Fig. 1. Schematic diagram of the double-recessed PHEMT used. Source-drain distance (L_{ds}), source-gate distance (L_{sg}), source-recess distance (L_{sr}), recess width (W_r), gate length (L_g), and gate foot-channel distance = Schottky layer thickness (D_s) are indicated. Their ranges of numerical values are given in Table I.

The vertical structure was determined by both varying the AlGaAs Schottky layer thickness—D_s from 18 nm to 26 nm and the carrier sheet density—n_s from 3×10^{12} cm^{-2} to 3.6×10^{12} cm^{-2}. The latter was measured by the wafer suppliers, IQE, Inc., using Hall measurements. To model the effect of the vertical geometry and doping level on the breakdown, a device matrix, comprising 14 identical devices, was defined. It is referred to as the "uniform matrix." The uniform matrix was defined at five different sites on the same mask set, to enable control of the process stability. Identical uniform matrices were repeated on six wafers, grown with various ns and D_s.

The lateral geometrical parameters and their interactions have a complex effect on the breakdown. Therefore, the Design of Experiment (DoE) approach [12], [13] has been used to develop the breakdown model. The DoE method makes it possible to design a device matrix with different lateral geometrical parameters, such that correlations between the geometrical parameters and measured electrical characteristics can be statistically established.

The device matrix was designed by a two-level factorial DoE and consisted of 16 different devices with various combinations of lateral layout parameters. The matrix is referred to as a "Device Zoo." The variables for the Device Zoo were based on a combination of the key lateral layout parameters of the baseline 0.25 mm power PHEMT. The Device Zoo was designed such that the modeled electrical characteristics of the matrix would take into account the main effects and all the two-factor-interaction effects. For modeling purposes, two different Device Zoo matrices, DZ-1 and DZ-2, as well as a uniform matrix were defined on a mask set and fabricated on all six wafers under research. The layout parameters and dimension ranges are presented in Table I.

All measurements used a HP 4551B semiconductor analyzer and RF probes. The statistical analysis of the data was carried out using SAS software (JMP 4.0). The Medici 1999.4 software was used for simulation of the electric field in the PHEMT.

TABLE I
FIVE KEY LAYOUT PARAMETER RANGES FOR THE 16-DEVICE DEVICE ZOO MATRIX

L_{ds} [μm]	L_{dr} [μm]	L_{dg} [μm]	L_g [μm]	L_r [μm]
3 ÷ 6.5	0.2 ÷ 1.7	0.5÷ 5	0.1 ÷ 0.2	1.7 ÷ 5

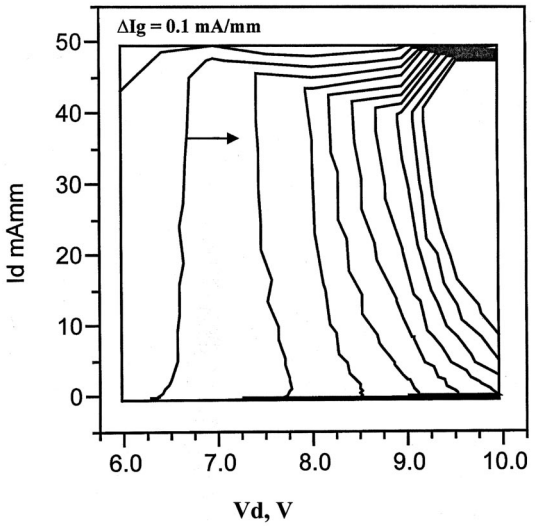


Fig. 2. Drain current (Id) as a function of drain voltage (Vds) at different constant gate currents from -0.12 mA/mm to -1.02 mA/mm with -0.1 mA/mm steps. Arrow shows the direction of Ig decrease. Rightmost contour ($Ig = -1.02$ mA/mm) limits the PHEMT safe operation region.

III. MEASUREMENTS, MODEL, AND PARAMETRIZATION

The common parameter, which characterizes the breakdown, is the breakdown voltage (Vb). A variety of criteria are used for extracting the breakdown voltage values. A straightforward one would be a sharp rise of the current, at a voltage corresponding to the breakdown voltage. However, reaching this point results in device degradation or burnout. Thus, indirect methods of breakdown voltage measurements have been proposed. Mostly, they use the following physical assumptions [7], [9]:

1) generation processes are responsible for the breakdown;
2) part of the generated carriers flow through the gate causing an increase of the gate current—Ig, which can be used as a "fingerprint" of the generation in the channel.

Our research also uses these assumptions. For complete breakdown characterization, we used a three-terminal measurement, where drain-source voltage—Vds was changed from 5 V to 16 V with 0.25 V steps, at each of which the drain current—Id and gate current—Ig were measured for gate-source voltage—Vgs between 0.5 V and -4 V (with 0.25 V steps). This measurement makes it possible to simultaneously determine all four basic transistor characteristics (currents and voltages at gate and drain) and then obtain different cross sections for analysis. Fig. 2 shows Id as a function of Vds in the form of constant Ig contours, similar to the presentation proposed in [7] to trace the transistor breakdown. The gate current—Ig changes from -0.12 mA/mm–1.02 mA/mm with -0.1 mA/mm steps. The arrow shows the direction

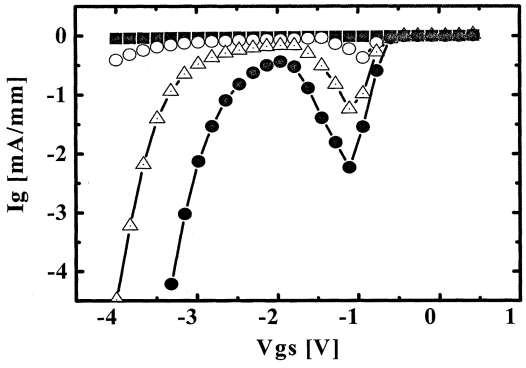


Fig. 3. Gate current (Ig) as a function of gate-source voltage (Vgs) at different constant drain voltages: $Vds = 6$ V (full squares), 10 V (open circles), 12 V (triangles), 15 V (full circles), and for PHEMTs on W2.

of Ig decrease. The unsafe operation range can be easily identified using this presentation. For this particular PHEMT, Fig. 2 shows that it is the area to the right of the curve for $Ig < -1.02$ mA/mm, which corresponds to operating voltages higher than 9.5 V.

To explore the physics of the breakdown and its correlation with geometrical parameters, another cross section, this time Ig (Vgs) at constant Vds was taken. Fig. 3 shows several Ig versus Vgs curves, at several values of Vds: 6 V (squares), 10 V (open circles), 12 V (triangles), and 15 V (full circles). While the gate-source voltage is ramped up from -4 V to 0.5 V, the gate current shows a Schottky diode behavior at drain-source voltages below 6 V. Analysis of the forward part of the curves shows that the gate diode has a 0.7 eV Schottky barrier and 1.4 ideality factor, which are in agreement with a benchmark [14]. For Vds above 6 V, a characteristic current peak occurs in the vicinity of $Vgs \sim -1$ V. The complicated shape of the Ig–Vgs curve seems to be the result of an interplay between two physical processes, TFE and impact ionization [7], [9].

The TFE current and impact ionization current have different temperature dependence. The impact ionization current depends on the generation rate α and the operation conditions. Under usual operation conditions, the temperature dependence of the impact ionization current is dictated by the temperature dependence of α. This dependence has the opposite sign of the TFE temperature dependence. Thus, this different dependence may be used for distinguishing between the impact ionization and TFE current contributions. To understand the temperature dependence of each process, we need to explore the physics of both TFE and impact ionization currents.

When the electric field in a semiconductor is increased above a certain value, the carriers gain sufficient energy to excite electron-hole pairs by impact ionization. The dependence of the impact ionization induced current on the electric field and the temperature can be written as [7], [10], [15]

$$I_{II} = \alpha \Delta L I_D \tag{1}$$

$$\alpha = A \exp\left(\frac{-TE_i}{V_{DG} - V_T}\right) \tag{2}$$

where I_{II} is the impact-ionization-induced current, α is the impact ionization rate, I_D is the drain current, ΔL is the length of the high field region at the gate end of the drain, A is a scaling constant, which depends on the device design, E_i is the ionization energy, T is the temperature, V_{DG} is the voltage between gate and drain, and V_T is the threshold voltage of the transistor. The impact ionization rate exponentially increases with increasing electric field between gate and drain and with decreasing temperature. The salient point of the equation is the temperature dependence of the impact ionization current.

The TFE induced gate current (I_{TFE}) is the sum of the thermionic emission (I_{TE}) and the tunneling (I_T) currents. The expression for I_{TFE} is given by [10]

$$I_{TFE} = I_{TE} + I_T = A \cdot T^2 \cdot \exp\left(-\frac{q \cdot \Phi_B}{kT}\right) \exp\left(\frac{q \cdot V}{kT}\right) + K' \cdot T \int_0^{\Phi_B} f_S(V) \cdot P(E) \cdot (1 - f_M)\, dE \tag{3a}$$

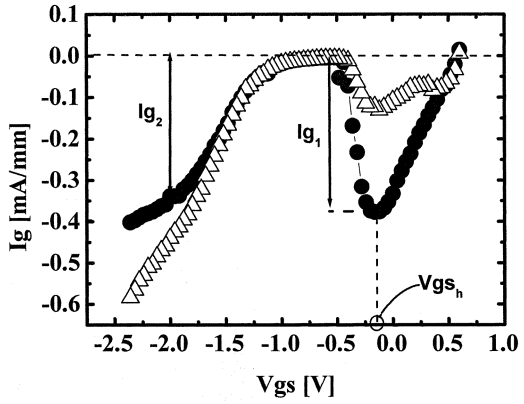
where I_{TE} and I_T are the thermionic emission current and tunneling current, respectively, Φ_B is the Schottky barrier height, $P(E)$ is the tunneling probability, A and K' are material coefficients while f_S and f_M are the Fermi-Dirac distribution functions for the semiconductor and the metal, respectively. At given operation conditions, the TFE induced current increases with increasing temperature, while the impact ionization current shows the opposite behavior because of the $\alpha(T)$ dependence.

Returning to Fig. 3, we note that $|Ig|$ sharply increases around $Vgs \sim -1$ V. This can be related to impact ionization [7]. Between -1 V and -2 V, Ig displays a negative differential resistance region, reflecting a decrease in the carrier density. The following current increase with increasing $|Vgs|$ is supposed to be due to TFE.

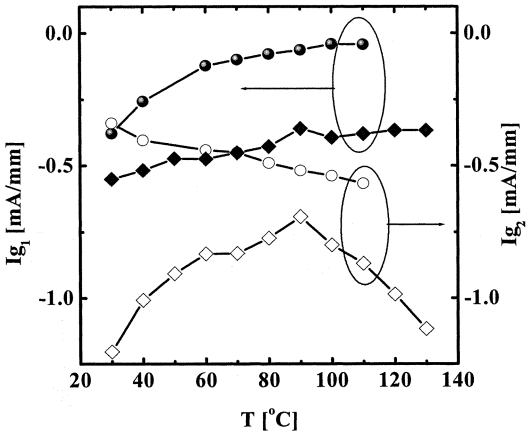
Since theory shows that impact ionization induced current and TFE have opposite temperature behavior, [10], [15], the two effects may be separated by temperature dependent measurements. Thus, we performed temperature-dependent measurements of the gate current in devices from a uniform matrix to experimentally examine the above hypothesis. The uniform matrix was measured on two wafers, W1 and W2, which differ by their Schottky layer thickness D_s and carrier sheet density n_s.

All 14 uniform matrix devices show similar Ig versus Vgs curves within any single vertical structure, while they differ from one structure to another. Fig. 4(a) shows typical Ig–Vgs curve at two different temperatures: room temperature (full circles) and 60 °C (triangles) for W1 vertical structure. The Ig (Vgs) curve can be divided into two regions: the current peak region—from 0.4 V to -0.5 V, where $|Ig|$ decreases with temperature; and the tail region from -0.5 V to -2.4 V, where $|Ig|$ increases with temperature. Therefore, two parameters have been selected to explore the temperature dependence the Ig (Vgs) curve: the height of the current peak Ig_1, which occurs at $Vgs = Vgs_h$ and a characteristic value of the second current increase, which is Ig $(Vgs = -2$ V)–Ig_2. The curve for W2 has similar features, but values of Ig_1, Ig_2, and Vsg_h are different. The values are presented in Table II.

Fig. 4(b) shows the current values Ig_1 (full symbols) and Ig_2 (open symbols) as a function of temperature for the two vertical structures—W1 (circles) and W2 (squares). In the case of W1, $|Ig_1|$ decreases from -0.37 mA/mm to -0.04 mA/mm with increasing temperature, indicating that this region is dominated



(a)



(b)

Fig. 4. (a) Gate current (Ig) as a function of gate-source voltage (Vgs) at room temperature (full circles) and at 60 °C (triangles) for PHEMTs fabricated on W1. Vgs_h, Ig_1 and Ig_2 are parameters. (b) Parameterized gate currents Ig_1 (full symbols) and Ig_2 (open symbols) as a function of temperature for the two vertical structures—W1 (circles) and W2 (squares).

TABLE II
Ig VERSUS Vgs CURVE PARAMETERS FOR TWO DIFFERENT VERTICAL STRUCTURES

	Ig_1, mA/mm	Ig_2, mA/mm	Vgs_h, V
V1	-0.37	-0.34	-0.04
V2	-0.52	-1.44	-1.1

by impact ionization. In contrast, $|Ig_2|$ increases with temperature from -0.34 mA/mm to -0.57 mA/mm, confirming that the tail current region is a result of TFE. The reduction of $|Ig_1|$ with temperature clearly indicates the Ig_1 governed by generation due to impact ionization [10], [15]. Thus, we can unambiguously distinguish between TFE and impact ionization and the current peak can serve as a fingerprint of impact ionization in the channel. Moreover, $|Ig_1|$ relates to the concentration of carriers, reaching the PHEMT gate, and therefore to the impact ionization rate. In general, $|Ig_1|$ is the sum of impact ionization and TFE currents, but as was shown in Figs. 3 and 4(a), the TFE current contribution in the current peak region is negligible. Thus, we can use $|Ig_1|$ as a monitoring parameter to explore the correlation between device geometry and impact ionization.

For the second structure W2, the current peak position—Vgs_h differs by almost 1 V, while the peak height Ig_1 shows a similar behavior to that of W1. Hence, Vgs_h is sensitive to the Schottky layer thickness and to the carrier sheet density and therefore, to the electric field distribution. It is interesting to note that for W2, Ig_2 shows a negative temperature dependence from RT to 100 °C and positive temperature dependence at temperatures above 100 °C. Apparently, the impact ionization contribution dominates in the tail region for this specific vertical structure at temperatures up to 100 °C while TFE becomes significant at higher temperatures.

In general, the current peak position and height reflect the impact ionization process in the PHEMT and are sensitive to the both Vds and Vgs, which form an electric field in the channel and Schottky layer. On other hand, the electric field distribution in the channel and Schottky layer is a function of the PHEMT lateral geometry and vertical design. Therefore, taking $|Ig_1|$ and Vgs_h as the current peak parameters, it is possible to empirically model the influence of the PHEMT geometry on impact ionization and relate the former to a safe operation region. The values of $|Ig_1|$ and Vgs_h reflect the physical processes in the PHEMT. Vgs_h characterizes Vgs (at a given Vds), for which the electric field in the channel reaches a value—Ec, causing maximum impact ionization current.

According to (1), the impact ionization current depends on I_D and α. I_D is defined by channel electron concentration n and electron drift velocity v. The n is controlled by gate voltage while v is controlled by the Vds. For less negative Vgs, I_d is high because of high n. However, the electric field at the gate end of the drain is low that results in lower impact ionization current. On the other hand, a large negative Vgs results in high α and lower n and I_D that cause low impact ionization current. Therefore $|Ig_1|$, maximizes for a certain combination of Vgs and Vds. Hence, the parameters affecting impact ionization form a multidimensional space, comprising lateral and vertical dimensions of the device as well as bias voltages. To understand the main dependencies, models, reflecting the influence of geometry on impact ionization at different bias voltages, have been built. As the DoE has been done for lateral geometry only, the models for lateral and vertical geometry effect on impact ionization have been developed separately. The empirical model, developed for $|Ig_1|$ and Vgs_h, characterizes the impact ionization phenomena in the PHEMT and can be used for optimization of the PHEMT power performance.

IV. EMPIRICAL IMPACT IONIZATION MODELS

A. Vertical Model

There are 336 (14 devices $\times$ 5 sites $\times$ 6 wafers) devices with identical layout parameters that have been measured on six wafers with different vertical structures to insure the statistical reliability of the results and to model the effect of the vertical geometry on impact ionization. The vertical structures differ by the electron sheet density $n_s = 3 \div 3.6 \cdot 10^{12}$ cm^{-2} and the Schottky layer thickness $D_s = 18 \div 26$ nm. The pinch-off voltage—Vp and saturation current at zero source-drain bias—$Idss$ correlate for all six structures with correlation coefficients of no less than 0.9. Such high coefficients indicate high consistency of the experiment and absence of measurement artifacts.

Measurements and parameterization of the $Ig\ (Vgs)$ curve have been done according to the scheme described in the previous section. Three $Ig\ (Vgs)$ cross sections at constant $Vds =$ 8, 10, and 12 V were taken. The Schottky layer thickness and carrier sheet density are representatives of the device vertical structure. The actual value of the Schottky layer thickness is difficult to extract, since it is defined by nonselective wet etching during the double-recess process and controlled by the current. Therefore, $Idss$ is selected as a natural representative of the Schottky layer thickness.

A stepwise regression approach [16] has been used for the modeling. It is an empirical technique, providing selection of a parameter or term for a model requiring little theoretical insight. For a regressor term to be considered in the model it has to have a significance probability value of 0.25 at least.

The general form of the equation describing the effect of the model terms ($Idss$ and n_s, in our case) on the modeled parameters (Vgs_h and Ig_1, in our case) is given by

$$\Phi = A_0 + \sum_n A_n \cdot P_n + \sum_{n,m} B_n \cdot P_n \cdot P_m \qquad (3b)$$

where Φ is the modeled parameter, P_n and P_m are the model terms and A_n and B_n are correlation coefficients.

Three models for three Vds values of 8, 10, and 12 V for each value of Vgs_h and $|Ig_1|$ have been built, with $Idss$ and n_s as the model terms. The models show a very good agreement with the measured Vgs_h in 80 ÷ 90% of the devices [see Fig. 5(a)], i.e., they reflect well the dependence of this parameter on the model terms. However, the model does not fit $|Ig_1|$ with a high level of confidence. The difference between the models for Ig_1 and Vgs_h demonstrates that the vertical geometry dominates Vgs_h but weakly affects Ig_1.

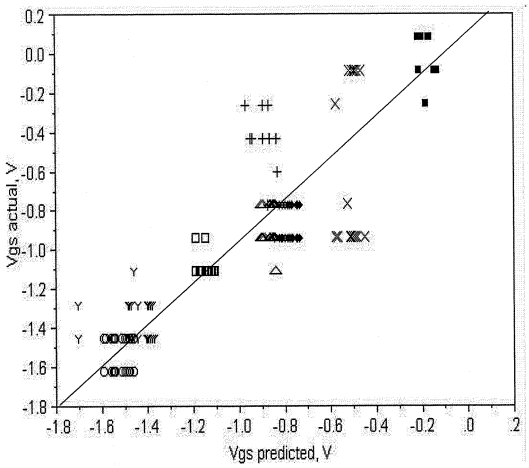
The Vgs_h models show a similar behavior of Vgs_h as a function of $Idss$ and n_s for all three Vds values and are explained by $Idss$ and n_s only, without any interactions. The expression of the model is given by

$$Vgs_h = A_o + A_1 \cdot Idss + A_2 \cdot n_s. \qquad (4)$$

The coefficients of the model are presented in Table III.

The main effect on Vgs_h is caused by $Idss$. According to the model, $|Vgs_h|$ increases with increasing $Idss$. This is because higher $|Vgs|$ is needed for reaching E_c in the channel due to the decrease of the electric field for larger D_s, corresponding to higher $Idss$. The effect of $Idss$ on Vgs_h is stronger than that of n_s. Increasing n_s causes a decrease of $|Vgs_h|$ because the electric field in the channel increases with n_s.

Thus, the vertical structure parameters define operating conditions, in which the breakdown most probably occurs. In the extreme cases of the model, PHEMTs fabricated on a structure with $Idss \approx 220$ mA/mm and $n_s \approx 3 \times 10^{12}$ cm^{-2} will experience impact ionization in the on-state, while PHEMTs defined on a structure with $Idss \approx 400$ mA/mm and $n_s \approx 3 \times 10^{12}$ cm^{-2} will be burned in the off-state at the same Vds. Since the two extreme structures have the same n_s and different $Idss$, the resulting modeled differences in Vgs_h indicate the dependence of the latter on the Schottky layer thickness D_s.



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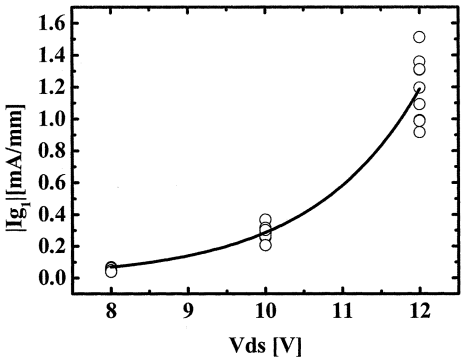

(b)

Fig. 5. (a) Predicted Vgs_h values as a function of actual Vgs_h values measured for all the investigated structures. Line shows best linear fit. (b) Impact ionization current $|Ig_1|$ as a function of drain-source voltage Vds for 16 Device Zoo devices of DZ-1. Solid curve is an exponential fitting.

TABLE III
VERTICAL MODEL COEFFICIENTS FOR THREE Vds VALUES

	Vds = 8 V	Vds = 10 V	Vds = 12 V
A_0 [V]	0.41	-1.7	-1.8
A_1, [10^{-3}·V·mm/mA]	-6	2	4
A_2, [10^{-13}·V·cm^2]	2	4	5

B. Lateral Model

The $Ig\ (Vgs)$ measurements for lateral modeling have been done on two Device Zoo matrices DZ-1 and DZ-2. To verify that the Ig_1 and Vgs_h distributions are affected by layout parameter changes rather than manufacturing process variations, the statistical distributions of Ig_1 and Vgs_h have been checked. Each distribution has been extracted from $Ig\ (Vgs)$ measurements on uniform and Device Zoo matrices under similar conditions, each containing 14 PHEMTs. The mean values and standard deviations are presented in Table IV. For the uniform matrix, deviations from the mean value are 9% for Ig_1 and 11% for Vgs_h, which are normal for a stable manufacturing process of HEMT [17]. For the Device Zoo matrices, the deviations from the Ig_1 mean values are higher for both matrices under study while there

TABLE IV
MEAN VALUE AND STANDARD DEVIATION OF Vgs_h AND Ig_1 FOR UNIFORM AND DEVICE ZOO MATRICES

	Uniform	DZ-1	DZ-2
Mean Value Vgs_h [V]	-0.84	-1	-0.87
Standard deviation for Vgs_h, %	11	0	11
Mean Value Ig_1 [mA/mm]	-0.06	-0.05	-0.09
Standard deviation for Ig_1, %	9	20	20

TABLE V
LATERAL MODEL COEFFICIENTS

Matrix	A_0	A_1 [$V^{-1}\cdot$]	A_2 [$\cdot\mu m^{-1}$]	A_3 [$\cdot\mu m^{-1}$]	A_4 [$\cdot\mu m^{-1}$]	B_{23} [$\cdot\mu m^{-1}$]	B_{34} [$\cdot\mu m^{-2}$]
DZ-1	-4.1	0.76	2.4	-0.88	-1.77	-3.5	5.81
DZ-2	-4.5	0.78	3.8	-0.76	-1.56	-3.3	4.46

is practically no deviation for Vgs_h (i.e., less than the measurement step, 0.04 V) for DZ-1 and for DZ-2. This indicates that Ig_1 strongly depends on the lateral geometry, whereas Vgs_h is not. This observation is in agreement with the theoretical considerations in Section III and verifies that only Ig_1 monitors the effects of the layout parameters on impact ionization.

Fig. 5(b) shows $|Ig_1|$ as a function of Vds for DZ-1. Each circle represents a measurement of a single PHEMT. The solid curve represents a calculated exponential fitting of $|Ig_1|$ as a function of Vds. The exponential dependence of the impact ionization induced current on the applied voltage shown by the measurements is according to (2). The data scattering reflects the influence of layout variation on $|Ig_1|$. To study this influence, a stepwise regression modeling was performed. A single model for $\ln|Ig_1|$ was constructed for DZ-1 and DZ-2 for the three values of $Vds = 8$, 10, and 12 V, together with the lateral layout distances. The expression of the model is given by

$$\ln|Ig_1| = A_0 + A_1\cdot Vds + A_2\cdot L_g + A_3\cdot L_{ds} + B_{23} \cdot L_g\cdot L_{ds} + A_4\cdot L_{dg} + B_{34}\cdot L_g\cdot L_{dg}. \quad (5)$$

The coefficients of the model are presented in Table V. The model is in agreement of 98% with the measured $\ln|Ig_1|$ with Vds as the only parameter, making it the most significant model term. It is also in agreement with (1).

Fig. 6 shows Vds, as predicted by the complete model [(5)], as a function of the measured $\ln|Ig_1|$ for each PHEMT. The shift of each predicted Vds from its measured value (8, 10, 12 V) shows the influence of the layout parameters (which are different for each device) on $\ln|Ig_1|$. The results indicate a gain about a volt in breakdown voltage by variation of the layout parameters.

Besides Vds, there are also the lateral geometrical parameters of the model, L_g, L_{gd}, and L_{sds}. The modeling shows that the term for the interaction between L_{dg} and L_{ds} is the most significant geometrical term of the model for any given matrix. Modeling DZ-1 and DZ-2 shows the same trend, with slightly different coefficients. Analysis of the model equation shows that

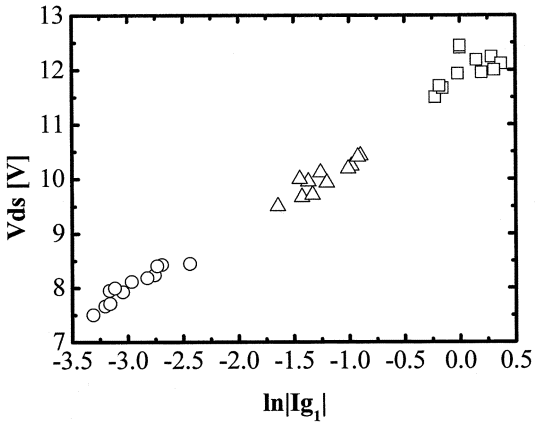

Fig. 6. Drain-source voltage Vds as a function of $\ln|Ig_1|$ as predicted by the model. Each cluster of points relates to a different Vds: 8 V (open circles), 10 V (triangles), and 12 V (squares).

from the impact ionization point of view there is an optimal position of the gate relate to the drain. When L_{gd} is about 1.6 μm, L_g an be vary between 0.1 μm and 0.2 μm without affecting the impact ionization induced current. It has been shown [18] that there is an optimal distance from the gate to the drain, which provides maximum output power.

The existence of the optimal gate position has a physical explanation, supported by numerical simulations of the electric field in the channel. Simulations performed by Dieci *et al.* [19] show that under certain conditions the electric field in the channel has two peaks—one at source side of the gate and another at the drain side. the channel region length, where the electric field is higher than E_c, ΔL is the distance where impact ionization occurs [see (1)], because the InGaAs (small band gap) channel is the weakest place from impact ionization point of view. According to the simulation results, ΔL can be situated fully between gate and drain or can consist of two parts: between gate and drain and between gate and source. In a HEMT with a central gate, ΔL is the distance between gate and drain. As the gate is shifted toward the source, ΔL decreases until the distance between gate and source becomes small enough to produce an electric field in the channel higher than E_C, i.e., the second region of ΔL. This point is the optimal gate position. Obviously, this position depends both on the drain-gate distance and the gate length under the same bias conditions. Our approach allows defining quantitatively the impact of the gate distance and the gate length on the optimal gate position for any given vertical HEMT epi-structure. the coefficients of interaction between L_{gd} and L_{ds}, and L_{gd} and L_g reflect the extent of the interplay between drain-gate and drain-source distances and between the drain-gate distance and the gate length, respectively (see Table V).

We obtain $L_{gd} = 1.6$ μm as the optimal distance for the given vertical structure, however, the set of measurements and modeling proposed in this paper can be used as a tool for optimal layout parameters definition for any vertical structure, application and operation conditions.

The correlation coefficient between the measured $|Ig_1|$ and the predicted values is 99%. The L_r and L_{dr} show minor effects of the model and slightly affect the impact ionization cur-

rent within given layout parameters. Therefore, figures of merit other than the breakdown voltage may be considered for decision about their dimensions within given ranges.

V. Conclusions

In summary, we have presented a systematic study of impact ionization in PHEMT, using the mapping measurement technique. Temperature-dependent measurements show that impact ionization is responsible for the characteristic current peak at Ig versus Vgs curve. A large number of careful measurements on specially designed Device Zoo and uniform matrices allow exploring the effect of both lateral and vertical PHEMT geometry as well as electron sheet density on impact ionization. Using the Device Zoo approach, empirical models for the impact ionization dependence on device geometry and sheet density were developed. The vertical model shows that impact ionization can occur in both the on-state and off-state of the PHEMT, depending on the initial wafer vertical design. Control of the lateral layout parameters enables designing PHEMTs with high output power and high breakdown voltages. We believe that the Device Zoo approach presented above can serve as an effective tool to adjust the layout parameters of given HEMT epi-structures for any system or application requirements.

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