Time-Dependent Dielectric Breakdown of 4H-SiC/SiO_2 MOS Capacitors

Moshe Gurfinkel, *Student Member, IEEE*, Justin C. Horst, John S. Suehle, *Senior Member, IEEE*, Joseph B. Bernstein, *Senior Member, IEEE*, Yoram Shapira, Kevin S. Matocha, *Member, IEEE*, Greg Dunne, and Richard A. Beaupre

***Abstract*—Time-dependent dielectric breakdown (TDDB) is one of the major issues concerning long-range reliability of dielectric layers in SiC-based high-power devices. Despite the extensive research on TDDB of SiO_2 layers on Si, there is a lack of high-quality statistical TDDB data of SiO_2 layers on SiC. This paper presents comprehensive TDDB data of 4H-SiC capacitors with a SiO_2 gate insulator collected over a wide range of electric fields and temperatures. The results show that at low fields, the electric field acceleration parameter is between 2.07 and 3.22 cm/MV. At fields higher than 8.5 MV/cm, the electric field acceleration parameter is about 4.6 cm/MV, indicating a different failure mechanism under high electric field stress. Thus, lifetime extrapolation must be based on failure data collected below 8.5 MV/cm. Temperature acceleration follows the Arrhenius model with activation energy of about 1 eV, similar to thick SiO_2 layers on Si. Based on these experimental data, we propose an accurate model for lifetime assessment of 4H-SiC MOS devices considering electric field and temperature acceleration, area, and failure rate percentile scaling. It is also demonstrated that temperatures as high as 365 °C can be used to accelerate TDDB of SiC devices at the wafer level.**

***Index Terms*—Reliability, time-dependent dielectric breakdown (TDDB), 4H-silicon carbide (SiC) MOS capacitors.**

I. Introduction

EXCELLENT material properties are possessed by 4H-silicon carbide (SiC) for high-temperature, high-frequency, and high-power applications. It has a wide bandgap (3.26 eV), a high thermal conductivity (more than twice higher than Si), a high critical field (2.2 MV/cm versus 0.25 MV/cm for Si), a high saturated drift velocity (higher than GaAs), and high thermal stability; it is chemical inert; and it forms a native oxide. Despite these beneficial properties, the current SiC MOSFET technology still suffers from performance and reliability problems that prevent its application for commercial power devices.

The reported channel mobility values of SiC MOSFETs with thermally grown SiO_2 are extremely and unacceptably low (less than 10 $cm^2/V \cdot s$). This poor mobility is attributed to the high density of traps at and near the SiO_2/SiC interface [1]. Postoxidation annealing of the gate oxide in nitric oxide (NO) or nitrous oxide (N_2O) seems to have considerably improved the device performance, and peak field-effect-mobility values of up to 50 $cm^2/V \cdot s$ have been reported [2]. Recently, a record peak field-effect mobility of 150 $cm^2/V \cdot s$ has been achieved after performing the oxidation process in the presence of alumina [3].

In spite of the considerable progress in device performance, reliability is still an important issue. One of the major reliability concerns is the instability of the threshold voltage in SiC MOSFETs under normal operation conditions. This instability is attributed to transient trapping of channel electrons in interface and bulk oxide traps [4]–[6]. Post oxidation annealing in NO has been shown to dramatically reduce this transient trapping, and the short-term reliability of NO-annealed MOS devices looks promising. On the other hand, it is unclear whether thermally grown silicon dioxide layers on SiC can reliably withstand the high electric fields and high temperatures over the desired long operating lifetime.

One of the major concerns for long-time reliability of dielectric layers in high-power devices is time-dependent dielectric breakdown (TDDB). Although the dielectric layer material in the SiC and Si MOS systems is identical (SiO_2), the barrier height between the SiC substrate and SiO_2 is much smaller. The reported conduction-band offset (ΔE_C) values between SiO_2 and 4H-SiC vary between 2.45 [7] and 1.92 eV [8] (0.65–1.18 eV lower than that for SiO_2 on silicon). The conduction-band offset controls the injection of electrons from the semiconductor to the oxide via Fowler–Nordheim tunneling. Thus, 4H-SiC exhibits a much higher tunneling current than in Si under similar applied fields. Indeed, Fowler–Nordheim tunneling has been suggested to contribute to dielectric breakdown, particularly at high electric fields [9]. Another variation is the incorporation of carbon species into the thermally grown SiO_2 layer [10]. Due to these intrinsic differences, in order to accurately assess the lifetime of SiC power MOS devices, it is highly important to find out whether SiO_2 dielectric layers on SiC behave similarly to comparable-thickness SiO_2 layers on Si. The oxide thickness in power devices is much thicker (> 50 nm) than those in modern Si devices in order to sustain the high gate voltages. Consequently, different breakdown mechanisms such as field-driven electron energy and positive charge generation are dominant. A good review of dielectric breakdown mechanisms in thick SiO_2 layers is given in [11].

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M. Gurfinkel and Y. Shapira are with the School of Electrical Engineering, Tel Aviv University, Tel Aviv 66978, Israel (e-mail: moshegur@post.tau.ac.il).

J. C. Horst and J. S. Suehle are with the Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD 20899 USA.

J. B. Bernstein is with Bar-Ilan University, Ramat-Gan 52900, Israel, and also with the Department of Mechanical Engineering, University of Maryland, College Park, MD 20742 USA.

K. S. Matocha, G. Dunne, and R. A. Beaupre are with the Semiconductor Technology Laboratory, General Electric Global Research, Niskayuna, NY 12309 USA.

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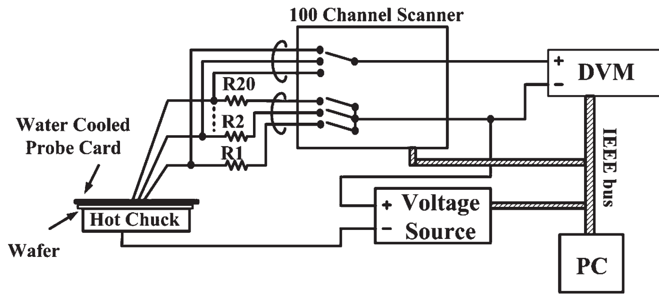

Fig. 1. Schematic diagram of wafer level constant voltage stress system. The system is capable of stressing 20 devices simultaneously at temperatures as high as 400 °C.

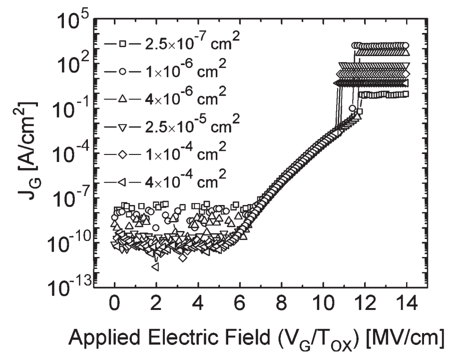

Fig. 2. Current density as a function of the electric field across the oxide of 4H-SiC capacitor with various areas at room temperature.

While there is extensive research on TDDB of SiO_2 layers on Si, there are only a handful of publications about TDDB of SiO_2 layers on SiC and there is a lack of high-quality statistical data. Maranowski and Cooper [12] presented constant voltage TDDB measurements on steam oxides on 6H-SiC. While their data sets show a large extrinsic failure population, extrapolations from the intrinsic populations predict a mean-time-to-failure (MTTF) of 100 years at 240 °C and 3 MV/cm, with a field acceleration parameter of 2.3 cm/MV. By using only one or two measurements per electric field, Lipkin and Palmour [13] measured time-to-breakdown on dry oxide 6H-SiC samples at 350 °C, estimating an MTTF of 3 h at 3 MV/cm and a field acceleration factor of 2.3 cm/MV. Krishnaswami *et al.* [14] compared constant voltage TDDB measurements of n-type MOS capacitors with the reliability of 4H-SiC DMOSFETs, suggesting that both have extrapolated lifetimes greater than 10^{10} h at 3 MV/cm and 175 °C. These capacitor and DMOSFET results, measured at fields greater than 8.5 MV/cm, indicate a field acceleration factor of approximately 4.6 cm/MV. Recently, Matocha *et al.* [15] showed that field acceleration parameter of 4H-SiC MOS devices at temperature of 200 °C abruptly changed at electric fields higher than 8.5 MV/cm. The extrapolated lifetime based on these high electric fields overestimated the normal operating condition lifetime.

In this paper, we present comprehensive TDDB data of 4H-SiC capacitors with a SiO_2 gate insulator collected over a wide range of electric fields and temperatures. By using these experimental data, we propose an accurate model for lifetime assessment of 4H-SiC MOS devices considering electric field and temperature acceleration, area, and failure rate percentile scaling.

II. Experimental Setup

Silicon carbide MOS capacitors were fabricated on n-type epitaxial layers ($N_D = 10^{16}$ cm^{-3}) on 4H-SiC Si face wafers at 4° off-axis. These capacitors utilize a thick deposited field oxide and a ∼50-nm gate oxide grown by successive N_2O at 1250-°C and NO at 1175-°C thermal oxidations followed by deposition of a Mo gate using sputtering. The capacitors were rectangular in shape with active areas ranging from 25×10^{-8} up to 4×10^{-4} cm^2.

Fig. 1 shows a schematic diagram of a wafer level constant voltage stress system. The capacitors were tested simultaneously at the wafer level on a specially designed wafer probe station. This station features a water-cooled probe card and test fixture that allows testing up to 400 °C. A water jacket is attached to a ceramic probe card that removes the heat from the top of the card. All test devices are connected through a series resistor to a constant voltage source. The voltage is monitored across each device sequentially to determine if breakdown has occurred without interrupting the applied stress to the device. Once a failure is detected, the stress to that device is disconnected to ensure that the additional current flowing through failed devices does not interfere with adjacent devices under test. The system is capable of testing up to 20 devices simultaneously. In tests where the MTTF was shorter than 2000 s, devices were sequentially characterized to increase the test time resolution.

Initially, we had to verify that the fabrication process is uniform and that there are no edge or perimeter effects. Otherwise, it is impossible to compare results of capacitors of different areas. To accomplish that, we conducted voltage ramp tests on capacitors of all areas. The voltage ramp test followed the JEDEC standard procedure [16].

III. Results and Discussion

Fig. 2 shows the current density as a function of the electric field across the oxide of 4H-SiC capacitors with various areas at room temperature. The oxide thickness was 43 nm. All the curves are depicted on top of each other, and the breakdown fields are identical, within the error margin. These results confirm that the process is uniform and that we can compare devices of different areas.

In some tests, devices were characterized using a semiconductor parameter analyzer to accurately determine the current as a function of time. Fig. 3 shows the current density as a function of time of 4×10^{-4}-cm^2 4H-SiC capacitors with a 24-nm thick oxide. The temperature was 230 °C, and the applied electric field was 8.5 MV/cm. The current density curves are typical of thick oxide MOS capacitors under a constant voltage stress. The current continuously decreases due to electron trapping until the dielectric layer breaks down and the current abruptly increases. Some of the devices had failed earlier due to defect-induced failures and were removed from the rest of the analysis.

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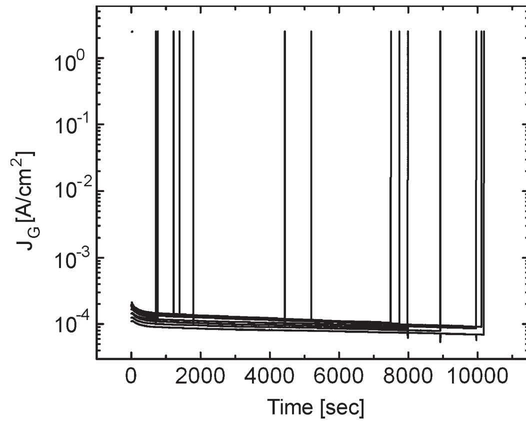

Fig. 3. Current density as a function of time of 4×10^{-4}-cm^2 4H-SiC capacitors with a 24-nm-thick oxide. The temperature was 230 °C, and the applied electric field was 8.5 MV/cm.

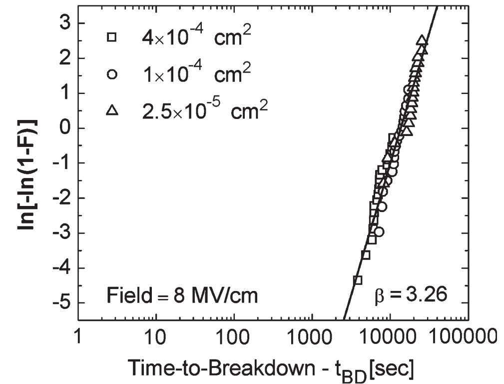

Fig. 4. Weibull distributions of 4H-SiC capacitors with three different areas (4×10^{-4} cm^2—squares, 1×10^{-4} cm^2—circles, and 2.5×10^{-5} cm^2—triangles). The results are normalized with respect to the 2.5×10^{-5}-cm^2 capacitor area.

A. Statistical Distribution and Area Scaling

In the past, dielectric breakdown was characterized using log-normal statistics. As the oxide layers became thinner ($t_{\rm ox} < 5$ nm), it was found that the percolation model [17] and the ensuing Weibull statistics described the TDDB breakdown statistics much better. The benefit of using the percolation model is that it allows area scaling. Equation (1) describes the Weibull relationship

$$\ln\left(-\ln(1-F)\right) = -\beta \cdot \ln(\alpha) + \beta \cdot \ln(t) \quad (1)$$

where F is the cumulative failure function, β is the shape parameter (or "Weibull slope"), and α is the scale parameter. The following equations describe the area and percentile scaling rules derived from the percolation model and Weibull statistics [18]:

$$\ln\left(-\ln(1-F_2)\right) - \ln\left(-\ln(1-F_1)\right) = \ln\left(\frac{A_2}{A_1}\right) \quad (2)$$

$$\frac{t_{\rm BD1}}{t_{\rm BD2}} = \left(\frac{A_2}{A_1}\right)^{1/\beta} \quad (3)$$

$$\frac{t_{{\rm BD}-F}}{t_{{\rm BD}-63\%}} \cong \left(\frac{F}{F_{63\%}}\right)^{1/\beta} \quad (4)$$

where $t_{\rm BD}$ is the time of breakdown and A is the oxide area. In Weibull analysis, $t_{63\%}$ is typically used, rather than the MTTF. This is the time at which 63.2% of the population has failed and is called the Weibull characteristic time.

In thick oxides, the percolation model may not be valid. However, Weibull statistics can theoretically describe any "weakest link" mechanism, even in the thick oxide case. Due to the lack of reported Weibull results of thick oxides, we had to first verify that TDDB of thick oxides does fit the Weibull statistic and its area scaling rules. Fig. 4 shows the Weibull distributions of 4H-SiC capacitors with three different areas (squares—4×10^{-4} cm^2, circles—1×10^{-4} cm^2, and triangles—25×10^{-6} cm^2). The curves are normalized with respect to the 25×10^{-6}-cm^2 capacitor. The obtained failure distributions, after area scaling, produce a single linear curve. This result

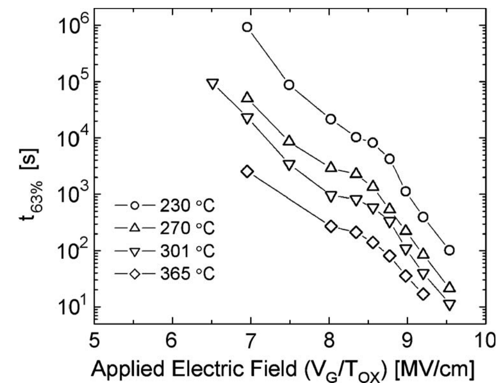

Fig. 5. $t_{63\%}$ as a function of applied electric field of 4×10^{-4}-cm^2 4H-SiC capacitors at different temperatures ranging from 230 °C to 365 °C. The gate oxide thickness was 43 nm.

confirms that Weibull statistics and area scaling rules are valid for thick oxide characterization. However, the extracted Weibull slope β is much lower than the prediction of the percolation model when considering the experimentally determined values of β for thinner oxides. The measured β values in this paper varied in the range of 3–10.

Both log-normal (not shown here) and Weibull statistics fit well the breakdown results of these thick oxide devices. For some of the results, log-normal fits better, but mostly Weibull statistic gives a better fit. The advantage of using the Weibull is the ability to perform area scaling. If log-normal statistics had been used, lifetime projection to larger area devices and chips would not be possible.

B. Electric Field Acceleration

We used the thermochemical "E model," $t_{63\%} \propto \exp(-\gamma E)$, to model the electric field acceleration [19]. To find the electric field acceleration parameter (γ), $t_{63\%}$ was extracted from the Weibull plots and plotted as a function of the applied electric field. Fig. 5 shows the $t_{63\%}$ as a function of the applied electric field of 4×10^{-4}-cm^2 4H-SiC capacitors at different temperatures ranging from 230 °C to 365 °C. The gate oxide thickness was 43 nm. Each point on the graph is extracted from a distribution of between 20

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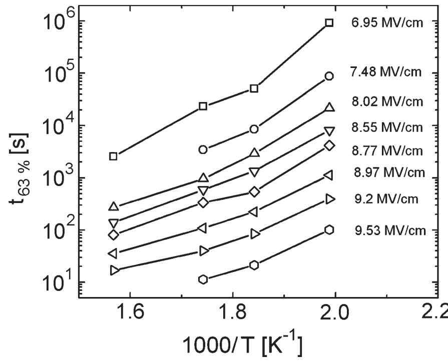

Fig. 6. $t_{63\%}$ as a function of 1000/T of 4×10^{-4}-cm^2 4H-SiC capacitors for different applied electric field values. The gate oxide thickness was 43 nm.

and 60 failed devices. There are two different regions in the field acceleration plot. At high electric fields, the acceleration parameter is about 4.6 cm/MV, whereas at low electric fields, the acceleration parameter is between 2.07 and 3.22 cm/MV. If we convert γ, in the lower field range, into an effective dipole moment: $P_{\text{eff}} = K_B T \times \gamma = 11.3 - 14.0 \ e\text{Å}$, then the data agree extremely well with the value of $\sim$13 eÅ, which is widely reported for silica-based dielectrics at low electric fields [20]. The point where the slope changes in the plot is at about 8.5 MV/cm. It is clear that another failure mechanism may become dominant at high electric fields. Matocha *et al.* [15] demonstrated this phenomenon at a single temperature of 200 °C. The results in Fig. 5 show that this phenomenon is temperature independent at the range of 230 °C–365 °C. Matocha *et al.* suggested that either increased Fowler–Nordheim tunneling or impact ionization was the possible cause for the abrupt change in the field acceleration. Schlund *et al.* [9] have shown that Fowler–Nordheim tunneling causes a similar effect in SiO_2/Si MOS devices at electric fields above 11 MV/cm. Because of the smaller conduction-band offset between SiO_2 and SiC, Fowler–Nordheim is expected to dominate in much smaller fields. Arnold *et al.* [21] have shown that the threshold electric field for impact ionization is thickness dependent and decreases from above 14 MV/cm for SiO_2 layers thinner than 10 nm down to about 8 MV/cm for 50-nm thick oxides. This is about the same electric field where we observe the change in the acceleration parameter.

This result is extremely important for lifetime extrapolation from accelerated tests. One should calculate the electric field acceleration factor from measurements conducted at fields lower than 8.5 MV/cm. Otherwise, the extrapolated value overestimates the real lifetime under normal operating conditions. To compensate for the use of lower electric fields and achieve a practical accelerated test length, the temperature must be accelerated furthermore. Fig. 5 shows that temperatures of up to 365 °C may be used to accelerate TDDB of 4H-SiC capacitors at the wafer level. Higher temperature stressing may also be feasible but has not been tested in this paper.

C. Temperature Acceleration

To find the temperature acceleration parameter, we took the data points from Fig. 5 and plotted $t_{63\%}$ in an Arrhenius plot.

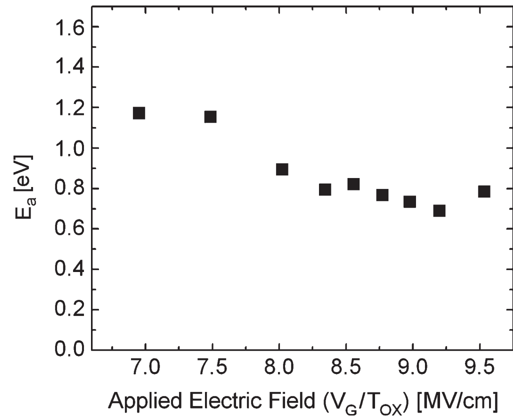

Fig. 7. Activation energy as a function of applied electric field of 4×10^{-4}-cm^2 4H-SiC capacitors.

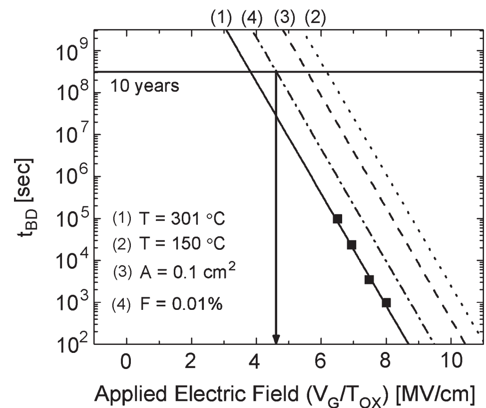

Fig. 8. Prediction of the maximum operating field for 43-nm-thick SiO_2 gate dielectric on top of SiC at low percentile failure rate of 0.01%. The squares represent measured failure data of 4×10^{-4}-cm^2 4H-SiC at an accelerated temperature of 301 °C. (1) The solid line is a linear fit of the logarithm of the time-to-breakdown (t_{BD}) as a function of applied electric field. The dotted lines represent the (2) lifetime projection for 150 °C, (3) total gate active area of 0.1 cm^2, and (4) low percentile failure rate of 0.01%.

Fig. 6 shows $t_{63\%}$ as a function of 1000/T of 4×10^{-4}-cm^2 4H-SiC capacitors for different applied electric field values. The gate oxide thickness was 43 nm. For all the electric fields, the curves are not perfectly linear and seem to have a slight curvature. This suggests that activation energy is not exactly constant with temperature. However, within acceptable error margins, the temperature acceleration can be described using the Arrhenius model, $t_{\text{BD}} \propto \exp(-E_a/kT)$, for a wide range of temperatures and electric fields. Fig. 7 shows the activation energy, extracted from Fig. 6, as a function of the applied electric field of 4×10^{-4}-cm^2 4H-SiC capacitors. The extracted activation energy shows a weak dependence on the electric field and is about 1.1 eV for an electric field of 7.0 MV/cm, a result that has been obtained for thick SiO_2 layers on Si in previous studies [22].

D. Lifetime Projection

Fig. 8 shows an example of how to extrapolate the lifetime under usage conditions from the accelerated conditions test results. The projection process takes into consideration the

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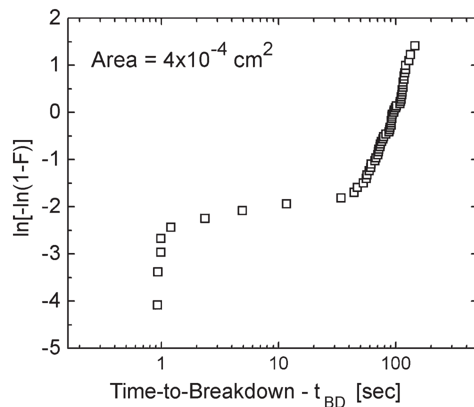

Fig. 9. Uncensored Weibull distribution of 4×10^{-4}-cm^2 4H-SiC capacitors at a temperature of 230 °C and under electric field of 8.9 MV/cm.

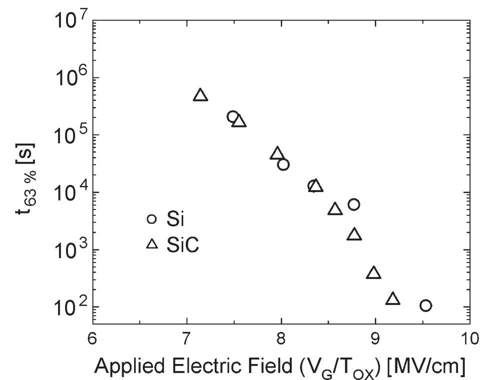

Fig. 10. $t_{63\%}$ as a function of applied electric field of 1×10^{-4}-cm^2 SiO$_2$ on Si capacitors (triangles) and SiO$_2$ on SiC capacitors (circles) at temperature of 230 °C. The gate oxide thicknesses were 50 and 43 nm, respectively.

electric field acceleration, temperature acceleration, area, and percentile scaling. The squares represent the measured failure data of 4×10^{-4}-cm^2 4H-SiC at an accelerated temperature of 301 °C. The solid line is a linear fit of the logarithm of the time-to-breakdown (t_{BD}) as a function of applied electric field. The dotted lines represent the lifetime projection for 150 °C, total gate active area of 0.1 cm^2, and low percentile failure rate of 0.01%. It is projected that the maximum tolerable operating electric field is 4.6 MV/cm for a 43-nm-thick gate dielectric at 150 °C with a ten-year TDDB lifetime. However, if the temperature is increased to 250 °C, the maximum tolerable operating electric field is reduced to 2.9 MV/cm (not shown here).

The temperature acceleration factor was calculated using an activation energy (E_a) of 1 eV, and a Weibull slope (β) value of three was used for the area and percentile scaling factors calculation.

E. Extrinsic Population

The models used in this paper describe only the *intrinsic* failure distribution. These failures are due to the intrinsic material properties of the SiO$_2$/SiC system. This is the case when the fabrication process is perfect and lacks any preexisting defects. Unfortunately, the present state-of-the-art fabrication processes of SiC power devices are far from perfect. The density of *extrinsic* defects is still unacceptably high. Fig. 9 shows the complete Weibull distribution of 4×10^{-4}-cm^2 4H-SiC capacitors at a temperature of 230 °C and an electric field of 8.9 MV/cm. The data set in this figure had a relatively high percentage of extrinsic failures and was thus chosen to demonstrate the problem. The average ratio of extrinsic failures for the 4×10^{-4}-cm^2 capacitors was about 5%. The extrinsic defect population follows the Poisson distribution with area size. Commercial power devices, such as IGBTs and DMOSFETs, have a much larger active area than the devices we used in this paper. Even if we can find the optimal temperature and field for long operation lifetime safe of intrinsic failures, the effective device lifetime will be dominated by the high density of extrinsic defects. Thus, further work is required to improve the fabrication process of SiC power device.

F. Material Considerations

To study the differences regarding the TDDB failure mechanism between the Si$-$SiO$_2$ and the SiC$-$SiO$_2$ systems, we compared capacitors fabricated on Si and on SiC substrates with similar oxidation process. Fig. 10 shows the $t_{63\%}$ as a function of applied electric field of 1×10^{-4}-cm^2 capacitors at temperature of 230 °C. The square symbols represent SiO$_2$ on Si capacitors, and the circles represent SiO$_2$ on SiC capacitors. The gate oxide thicknesses were 50 and 43 nm, respectively.

For applied electric fields below 8.5 MV/cm, both Si and SiC devices exhibit similar intrinsic failure times and electric field acceleration. This is not surprising since the oxide is SiO$_2$ for both cases, and the "E-model" [19], which is used to describe TDDB in thick oxides, predicts that the oxide failure time depends only on the applied electric field, regardless of the oxide thickness. Furthermore, Ogawa *et al.* [23] have shown that while carbon incorporation into SiO$_2$ films has a major impact on the oxide strength, it has little or no effect on the observed field acceleration parameter—γ.

However, at higher fields, the electric field accelerations of Si and SiC devices are different. In the previous section, we have shown that the failure mechanism changes at fields above 8.5 MV/cm. Increased F-N tunneling and impact ionization were considered as a cause of the change in the field dependence at high electric fields. This may explain the difference between Si and SiC at high electric fields since both phenomena strongly depend on the conduction-band offset (ΔE_C) and the oxide thickness.

Even though Si and SiC devices have similar $t_{63\%}$ values at electric fields below 8.5 MV/cm, there is a difference in their statistical distribution. For a given electric field, the Weibull slope parameter (β) of SiC devices is only half of the Si. These lower β values may be attributed to the high density of preexisting traps in the SiC$-$SiO$_2$ system. According to Sune's percolation theory [17], the gate oxide is modeled as a 3-D array of cells. The size of the cells (a_0^3) represents the "sphere of influence" of a single defect. During the stress period, defects are randomly created in these cells. Breakdown occurs as soon as a column of cells is fully defective inducing a conductive path through the oxide. Sune has shown that the Weibull slope

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(β) is proportional to the number of cells in one column—$\beta \propto t_{\mathrm{ox}}/a_0$. At the poor SiC/$SiO_2$ interface, there is a high density of interface and near-interface preexisting traps, which may be treated as defective cells. If these traps are treated as defective cells, the "effective" number of cells in one column is smaller; thus, β is expected to be smaller.

From these results, it may be concluded that the reliability of SiC$-$$SiO_2$ technology due to TDDB is limited only by the quality of the oxide and the interface, and not by the intrinsic properties of the SiC.

IV. Conclusion

TDDB data are presented for 4H-SiC capacitors with SiO_2 gate insulator collected over a wide range of electric fields and temperatures. Weibull statistics and area scaling rules for thin oxides were found to accurately describe TDDB of thick oxides, with the exception of a lower β value than theoretically predicted. At low fields, the electric field acceleration parameter is between 2.07 and 3.22 cm/MV. At fields higher than 8.5 MV/cm, the electric field acceleration parameter is about 4.6 cm/MV, indicating a different failure mechanism present under high electric field stress. Thus, lifetime extrapolation must be based on failure data collected below 8.5 MV/cm. It was also demonstrated that temperatures as high as 365 °C can be used to accelerate TDDB at the wafer level. Higher temperature stressing may be feasible as well but has not been tested in this paper. Temperature acceleration follows the Arrhenius model with activation energy of about 1 eV, similar to thick SiO_2 layers on Si. Further work is required to improve SiC power device processing so that the high density of extrinsic defects is eliminated.

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Moshe Gurfinkel (S'07) received the B.Sc. and M.Sc. degrees (both cum laude) in electrical engineering in 2003 and 2005, respectively, from Tel Aviv University, Tel Aviv, Israel, where he is currently working toward the Ph.D. degree in electrical engineering.

He has recently participated in an exchange program at the University of Maryland, College Park, and has been a Guest Researcher with the Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD. His research interests include reliability and characterization of advanced microelectronic devices.

Justin C. Horst received the B.S. degree in electrical engineering from Grove City College, Grove City, PA, in 2008.

Over the past two years, between academic semesters, he has been researching the reliability of semiconductor electronics at the National Institute of Standards and Technology, Gaithersburg, MD.

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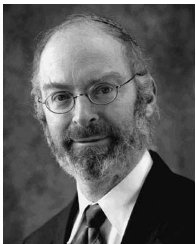
John S. Suehle (SM'95) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, in 1980, 1982, and 1988, respectively.

Since 1982, he has been with the Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD, where he is currently the Leader of the CMOS and Novel Devices Group. His research activities include failure and wear-out mechanisms in semiconductor devices, radiation effects in microelectronic devices, microelectromechanical systems, and metrology issues relating to future electronic devices. He is the author or a coauthor of more than 170 technical papers or conference proceedings. He is the holder of five U.S. patents.

Dr. Suehle serves as the chairman of the Oxide Integrity Working Group of the EIA/JEDEC JC 14.2 Standards Committee and is a member of Eta Kappa Nu. He serves as the Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES in the reliability area has served as Guest Editor of the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY. He holds positions on the management committees of the IEEE International Electron Devices Meeting, IEEE International Reliability Physics Symposium, and the IEEE International Integrated Reliability Workshop.



Joseph B. Bernstein (SM'03) received the Ph.D. degree in electrical engineering from Massachusetts Institute of Technology, Cambridge, in 1990.

He is a Professor of engineering with Bar-Ilan University, Ramat-Gan, Israel, and also with the Department of Mechanical Engineering, University of Maryland, College Park. He supervises the Laboratory for Laser Processing of Microelectronic Devices, Department of Materials and Nuclear Engineering, University of Maryland, and is the Head of the Microelectronics Device Reliability Program. He has been a Fulbright Senior Researcher/Lecturer and has set up a center for reliable electronics at Bar-Ilan University. This collaborative center serves the needs of industry through the cooperative research of academics and government agencies from Israel and the USA. His research areas include statistical interactions of multiple failure mechanisms in ULSI devices. He also extensively works with the semiconductor industry on projects relating to system qualification for reliability based on fundamental physics and circuit simulation techniques and on programmable devices and repair in microelectronic circuits and packaging. He is actively involved in microelectronics device and systems reliability research and physics of failure, including power device reliability, ultrathin gate oxide integrity, radiation effects, MEMS, and laser-programmable metal interconnect.

Yoram Shapira received the B.Sc. (with distinction) and D.Sc. degrees in physics from the Technion, Israel Institute of Technology, Haifa, Israel, in 1968 and 1973, respectively.

After three years as a Research Associate with the University of Wisconsin, he joined the Department of Electrical Engineering-Physical Electronics, Faculty of Engineering, Tel Aviv University (TAU), Tel Aviv, Israel, where he is currently a Full Professor and incumbent of the Henry and Dinah Krongold Chair of Microelectronics. He is currently on sabbatical at the University of Maryland, College Park. From June 1997 to May 1999, he was on a leave of absence for his appointment as the Science Minister-Counselor at the Embassy of Israel in Washington, DC, where he was elected as the President of the Science Diplomats' Club of Washington. He has held numerous university and faculty committee positions, including Director of the EE Undergraduate Program in 1999–2002, Chairman of the University Admission Committee in 1991–1994, EE Department Head in 1987–1991, and Member of the Steering Committee of the University Institute for Nano-Science and Technology of TAU in 1999–2003. He was the founder and first Director of the Wolfson Applied Materials Research Centre in 1994–1997 and 2000–2005 and the Director of the Gordon Center for Energy Research in 1996–1997 and 2000–2005. He has been a Visiting Scientist at several universities and institutes and has organized and chaired several conferences and symposia. He was the founder and first President of the Israeli Union of Materials (AGIL) in 1994–1997. He has coauthored more than 160 papers and book chapters, as well as more than 100 conference publications, and has supervised 56 graduate students and six postdoctoral students. His group currently comprises one postdoctoral student, three Ph.D. students, and three M.Sc. students, working on various characterization projects of electronic materials, nanostructures, devices, and organic/biointerfaces.

Dr. Shapira is a Fellow of the American Vacuum Society and an Honorary Member of the Israel Vacuum Society, having served as its Secretary in 1982–1989 and President in 1990–1992 and as the Israeli Representative and Councilor at the International Union for Vacuum Science (IUVSTA) for several terms.

Kevin S. Matocha (S'95–M'03) received the B.S. degree in electrical engineering from Louisiana Tech University, Ruston, in 1995 and the M.S. and Ph.D. degrees in electrical engineering from the Rensselaer Polytechnic Institute, Troy, NY, in 1998 and 2003, respectively. His doctoral work examined the capabilities of GaN MOSFETs for high-voltage switching applications.

Since 2000, he has been with the Semiconductor Technology Laboratory, General Electric Global Research, Niskayuna, NY, where he develops wide-bandgap devices, including SiC and GaN power transistors.

Greg Dunne received the B.S. degree in materials science and engineering from North Carolina State University, Raleigh, in 1996.

He was a Process Engineer with Northrop Grumman, Sterling Semiconductor, and Aixtron. He is currently a Process Engineer with General Electric Global Research, Niskayuna, NY, focusing on wide-bandgap materials growth and characterization.

Richard A. Beaupre received the B.A. degree in physics from Williams College, Williamstown, MA, in 1978 and the M.S. degree in electrical engineering and the M.E. degree in materials engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1979 and 1986, respectively.

Over the last 15 years, he has designed and developed electronic packaging solutions for various electronics applications, including power electronics. Prior to those assignments, he had worked for ten years in materials and process evaluation for General Electric Aerospace. He is currently a Packaging and Reliability Engineer with General Electric Global Research, Niskayuna, NY, where he is responsible for designing and fabricating advanced power modules for next-generation aerospace and industrial applications. This work includes reliability modeling of all interconnections within the power module and validating the failure modes with test data. He is also designing a test program and characterizing failure modes of power modules using combined environments—temperature, altitude, and humidity—for an aerospace application.

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