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Microelectronic Engineering 84 (2007) 2230–2234
MICROELECTRONIC ENGINEERING
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Characterization of electrically active defects in high-k gate dielectrics by using low frequency noise and charge pumping measurements

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Abstract

The electrically active defects in high-k/SiO_2 dielectric stacks are examined using a combination of low frequency noise (LFN) and charge pumping (CP) methods. The volume trap profile in the stacks is obtained by modeling the drain current noise spectra and charge pumping currents, with each technique covering a different depth range. The LFN is dependent on both the high-k and interfacial (IL) SiO_2 thicknesses while the CP current is mainly dependent on the IL thickness.

Keywords: low frequency noise, charge pumping, border trap, depth profiling

1. Introduction

Hafnium-based dielectrics are primary candidates as a replacement of SiO_2 for next generation complimentary metal-oxide-semiconductor (CMOS) devices. However, these materials exhibit a much higher defect density when compared to SiO_2, aggravating some major device reliability issues including time dependent dielectric breakdown and threshold voltage instabilities. It is apparent that the knowledge of the trap location and density (i.e., their spatial distribution) can improve the understanding of their effects on device reliability. Unfortunately, a consensus about the defect spatial profile has not been reached, especially for two-layer stack MOSFET devices comprising high-k dielectrics and interfacial SiO_2, although some limited information has been gathered mostly by using the charge pumping technique [1-3] and other methods [4, 5].

The low frequency noise properties, an important figure of merit for the dielectric quality [6-8], have not been studied thoroughly in the high-k/IL system.

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0167-9317/$ - see front matter Published by Elsevier B.V.
doi:10.1016/j.mee.2007.04.094

Charge pumping and low frequency noise measurements are natural complimentary techniques to characterize the electrically active traps in the dielectrics with the former caused by the traps closer to the substrate/dielectric interface [9] while typically low frequency noise covers deeper depths [10-12] if tunneling is assumed to be the dominant process.

In this work, the trap spatial profiles in the high-k layer for two-layer stacks are extracted from LFN and compared for wafers with different high-k thicknesses. The effects of scaling either the high-k layer or the IL thickness on the low frequency noise are studied. Volume trap profiles in this type of system are reported for the first time using a combination of 1/*f* noise and charge pumping methods, covering most of the region where the traps can actively affect the current transport in the channel.

2. Experimental details

The devices used in this work are fully processed MOSFETs with HfO_2 (HfSiO)/SiO_2 stacked gate dielectrics. High-k gate dielectric transistors were fabricated on 200 mm p/p+ epitaxial Si <100> wafers by using a standard CMOS process with 1000 ^{0}C 10 s dopant activation anneal.

Table 1.
Gate and dielectric information and parameters extracted from DC measurements

Gate Stack IL/HfO_2	Metal Gate	EOT (nm)	V_{th} (V)	V_{fb} (V)
1 nm/3 nm	TiN	1.28	0.78	-0.58
1.5 nm/3 nm	TiN	1.7	0.82	-0.56
2 nm/3 nm	TiN	2.1	0.89	-0.55
1 nm/7 nm	TiN	2.5	0.91	-0.7
1 nm/2 nm HfSiO	TaN	2.05	1.28	-0.15
3.3 nm/2 nm HfSiO	TaN	4.27	1.73	-0.1

DC measurements were performed with a semiconductor parameter analyzer to obtain static parameters. Capacitance-Voltage measurements were used to extract the equivalent oxide thickness (EOT). A constant amplitude charge pumping technique was utilized to measure CP current as a function of frequency. LFN measurements were performed using a standard noise measurement setup including two channel low noise DC biasing sources, a low noise voltage pre-amplifier, and a dynamic signal analyzer. The gate stack composition and thickness along with other parameters are listed in Table 1.

3. Results and discussion

Fig. 1 shows typical drain current noise spectra measured at different gate voltages for a nMOSFET with 7 nm HfO_2 /1 nm SiO_2 gate stack. Predominantly $1/f^{\alpha}$ like spectra are obtained with α equal to ~1.2. Trapping and detrapping of carriers tunneling from the inversion layer at the border trap sites causes LFN [13-15], with each tunneling depth corresponding to a specific time constant for the reversible charge exchange process following:

$$\tau = \tau_0 \exp(\alpha_t x) \quad (1)$$

where τ_0 is the time constant at the interface and x is the distance into the oxide from the Si-SiO_2 interface.

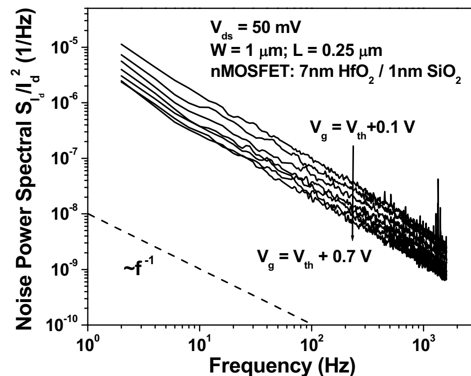

Fig. 1. Typical normalized current noise power spectrum density for device with 7 nm HfO_2/1 nm IL.

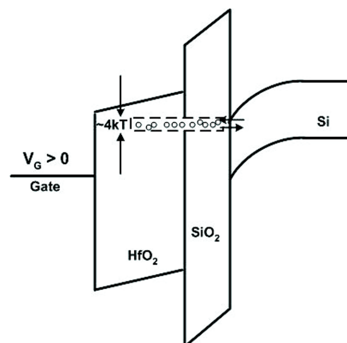

Fig. 2. Band diagram of a nMOSFET with two-layer dielectrics.

As illustrated in Fig. 2, depending on the thickness of the IL layer, the trap sites responsible for the LFN can be within the IL layer only, within the HfO_2 only, or both. The tunneling parameter α_t is governed by the effective mass of the electron in the dielectrics, m_e^*, and the barrier height from the Si conduction band edge to the dielectric conduction band edge, ϕ_B, with:

$$\alpha_t = \sqrt{\frac{2 m_e^* \phi_B}{\hbar^2}} \tag{2}$$

where $\hbar$ is Plank's constant divided by 2π. As a result, lower frequencies correspond to larger tunneling depths, away from the Si/IL interface. The well-established number fluctuation model can be used to calculate the volume trap density in the high-k layer by using the following formula [11]:

$$N_t = \frac{S_{Id} \alpha_t C_{EOT}{}^2 WLf}{g_m{}^2 q^2 kT} \tag{3}$$

where kT is the thermal energy, q is the elementary charge, C_{EOT} is the capacitance associated with equivalent oxide thickness, W is the channel width, L is the channel length, f is the frequency, S_{Id} is the spectral density of the current noise, and g_m is the transconductance. A uniform trap distribution would generate pure 1/*f* noise [10]; i.e., the frequency exponent α equal to 1.

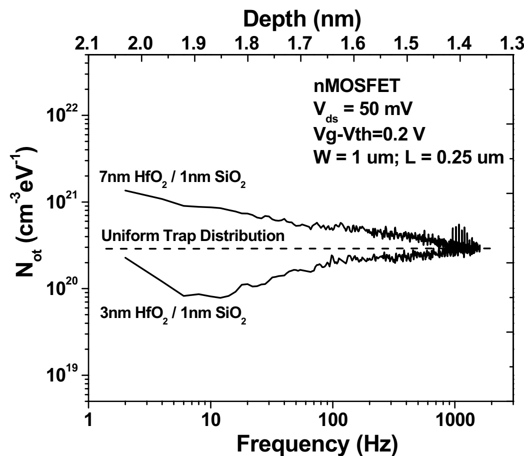

Fig. 3. Qualitative trap distribution profile at V_g-V_{th} = 0.2 V for two wafers with different high-k thickness

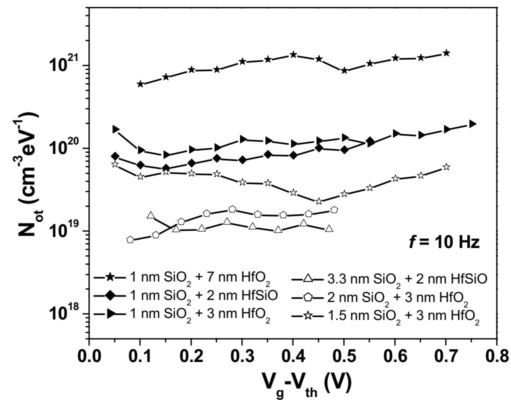

Fig. 4. N_{ot} extracted by LFN measurements for different gate stacks.

The frequency axis can be translated to the tunneling depth through Eqs. (1) and (2) by using the SiO_2 parameters. The noise spectra measured in devices with different HfO_2 thickness are converted to trapping density profiles, as shown in Fig.3. It should be noted here that the same frequency should correspond to a larger depth if the HfO_2 parameters are used instead of those for SiO_2. Nevertheless, the frequency range (1 Hz to 1.6 kHz) of the measurements should ensure that only the traps located in HfO_2 are probed in the devices with these two gate stacks whether HfO_2 or SiO_2 parameters are used. The inaccuracies this caused on defect density and depth determination does not affect the qualitative nature of this assessment, and are neglected in this work. It is obvious that the trap density for the 7 nm HfO_2 device increases from the HfO_2/IL interface to the HfO_2/TiN interface. For the 3 nm HfO_2 devices, in the bulk of the film, the trap density is essentially constant and then decreases until a "kink" appears at lower frequencies, supposedly close to the metal/HfO_2 interface. The observed decrease of the measured trap density with a deeper probing can be an indication of the real trap profile, although it cannot be ruled out that it may be caused by a higher rate of the electron detrapping to the gate electrode for the traps located close to the gate. It is unclear at this point what causes the kink. This comparison shows that scaling the high-k dielectric is a simple but very effective way to reduce the dielectric trap density and improve its performance.

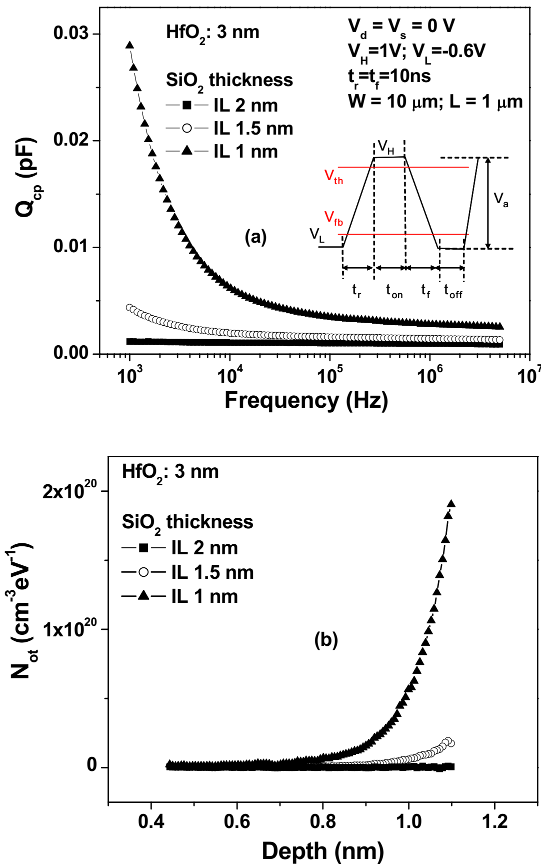

Fig. 5. (a) Charge pumped per cycle as a function of frequency for three wafers with different IL thicknesses. The set shows the parameters for the gate pulse and their values; (b) Qualitative trap profile from frequency dependent charge pumping.

N_{ot} extracted at 10 Hz in 6 wafers in Table 1 are compared in Fig. 4. Seven nm HfO_2 film devices have the highest trap density. The trap density is much lower for the two wafers with IL thickness greater than ~2 nm since the probing depth at f=10Hz does not extend beyond the SiO_2 layer. The two wafers with 1 nm IL thickness show comparable trap density with the thinner HfSiO film showing a slightly better dielectric quality. The wafer with 1.5 nm IL thickness has an intermediate trap density compared to those with 1 nm and 2 nm IL.

CP current is also measured as a function of frequency for three wafers with the same high-k thickness but varied IL thicknesses. Fig. 5 (a) shows the charge pumped per cycle (Q_{cp}) versus frequency in the range of 1 kHz to 5 MHz. The thinnest IL device has the higher Q_{cp}, because the “trappier” HfO_2 layer is closer to the substrate. Trap profiles are extracted from the CP data and are plotted in Fig. 5 (b) following [9]:

$$N_{ot}(x_m) = -\frac{1}{q\lambda_n A\Delta E_t}\frac{dQ_{cp}}{d\ln(f)} \tag{4}$$

where A is the gate area, Q_{cp} the charge pumped per cycle, f the measurement frequency, and λ_n the attenuation coefficient. The starting trap density values close to the SiO_2/Si interface are very similar for all dielectrics, suggesting a good interface quality. For devices with 2 nm IL, the trap density is low and constant in the SiO_2 within the range of probing depths of CP measurements. In the device with a 1 nm IL, the reaction between SiO_2 and HfO_2 raises the trap density in the IL, while the device with a 1.5 nm IL has an intermediate trap density.

Fig. 6 shows an example of combined qualitative trap profile of a wafer with 3 nm HfO_2/1 nm IL from both LFN and CP analysis. The trap density in the IL increase with closer proximity to the high-k layer, in agreement with earlier reports [16] and this effect

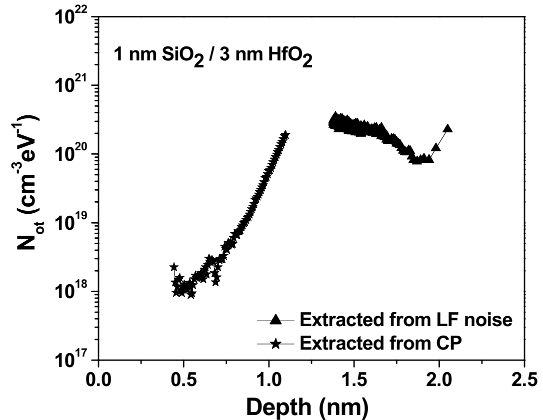

Fig. 6. Qualitative profile with noise and charge pumping. Test conditions are the same as Figs. 3 and 5.

was attributed to higher density of the high-k induced oxygen vacancies in the IL [17]. Despite the limitation of the probing depth for both techniques, especially the lower frequency end of the CP method due to leakage current and the higher frequency

portion of the LFN measurement due to the thermal noise starting to dominant and introducing error, this trap profile covers the majority of the region for the thin dielectric stacks where pre-existing border traps can electrically affect the DC parameters of the devices.

4. Conclusions

The combination of low frequency noise and charge pumping methods is used for the first time to obtain the volume trap profile for a large depth range where the traps can actively affect the current transport in the channel for state-of-the-art CMOS transistors with high-k/SiO_2 dielectric stacks. The noise is dependent on both the high-k and IL thicknesses. The charge pumping current is mainly dependent on the IL thickness.

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